To Keep or Not to Keep – The Volatility of Replacement Policy Metadata in Hybrid Caches

2nd Workshop on Disruptive Memory Systems (DIMES ’24), Austin, TX, USA

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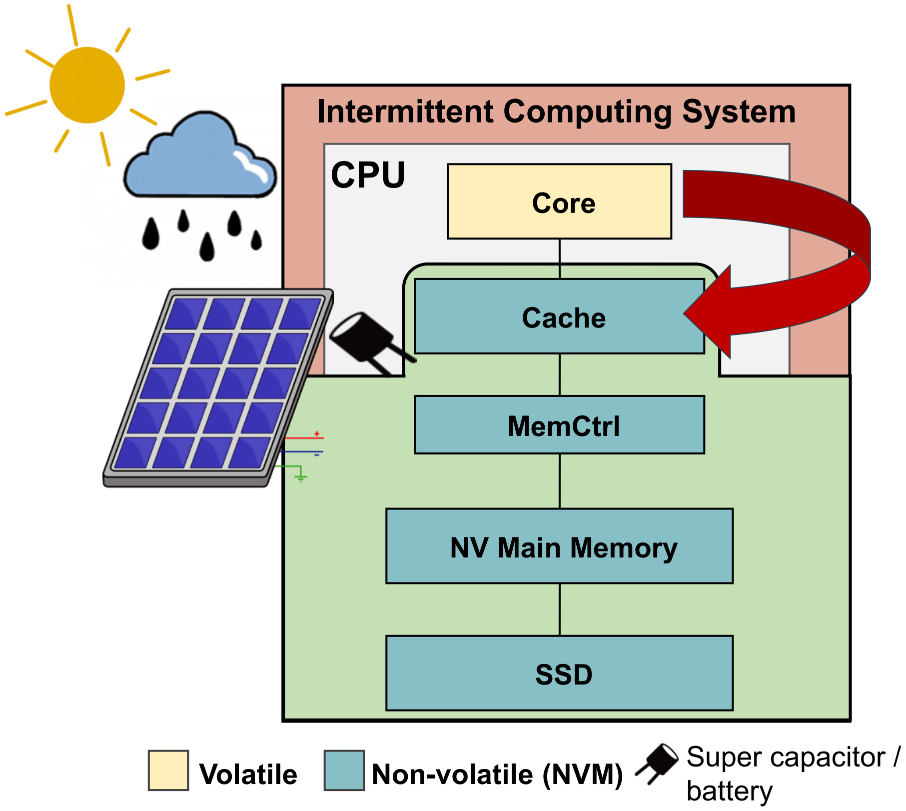
Introduction

Intermittent Computing

- IoT devices, wearables etc. powered by energy harvesting modules, e.g., solar panels

→ Unstable power supply

- System must not lose state and data due to a power shortage
- NVM technologies promise great potential for intermittently powered embedded systems



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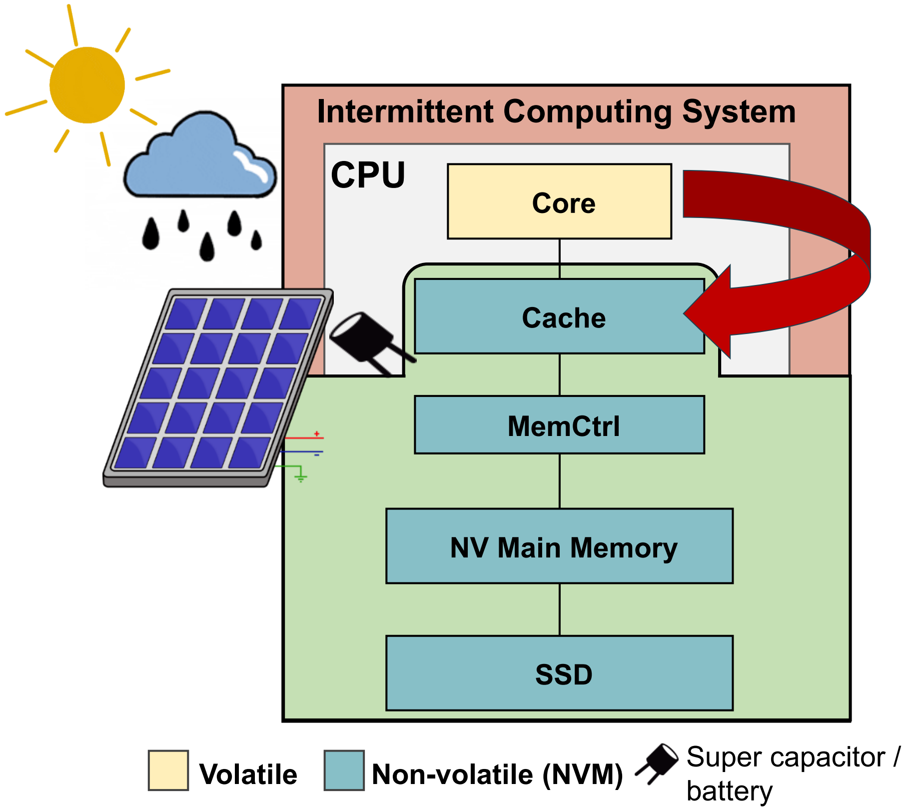
Instruction Level Persistence:

- Supply voltage below threshold → power outage detected
- Run currently issued instructions to completion
- Write back all volatile modified data to a persistent memory

→ Continue at instruction where execution was halted, once power is restored



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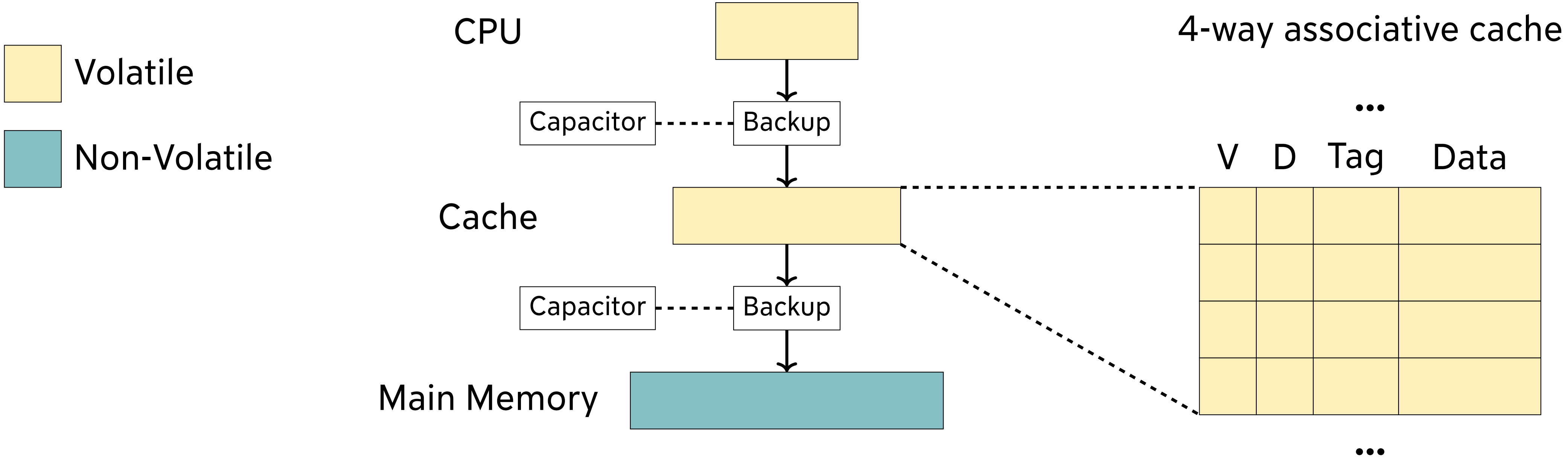
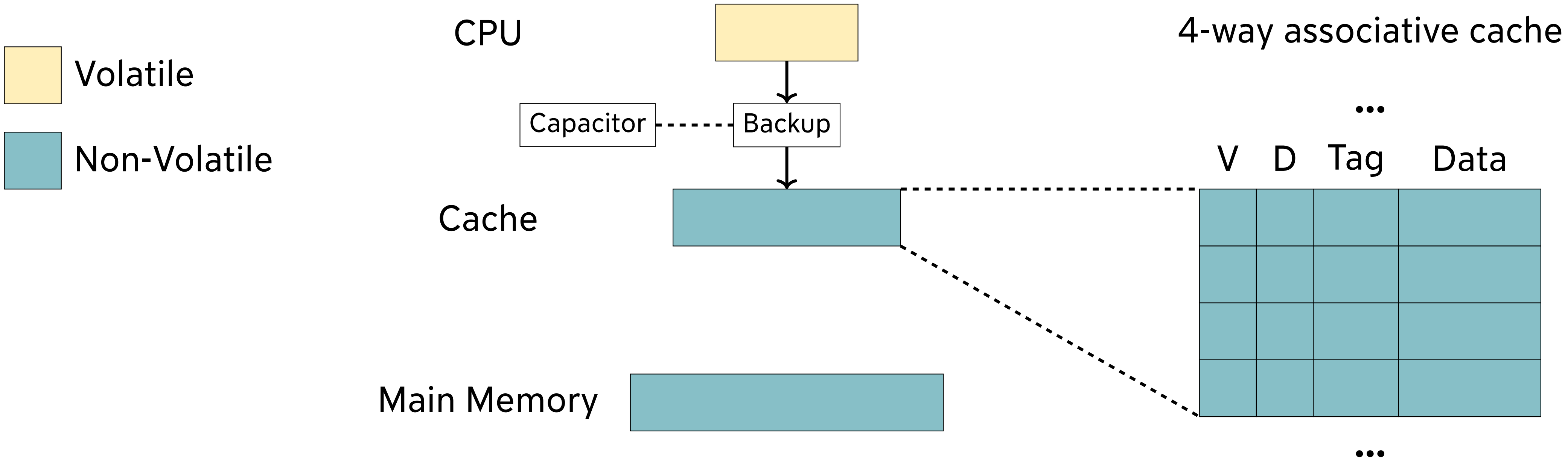
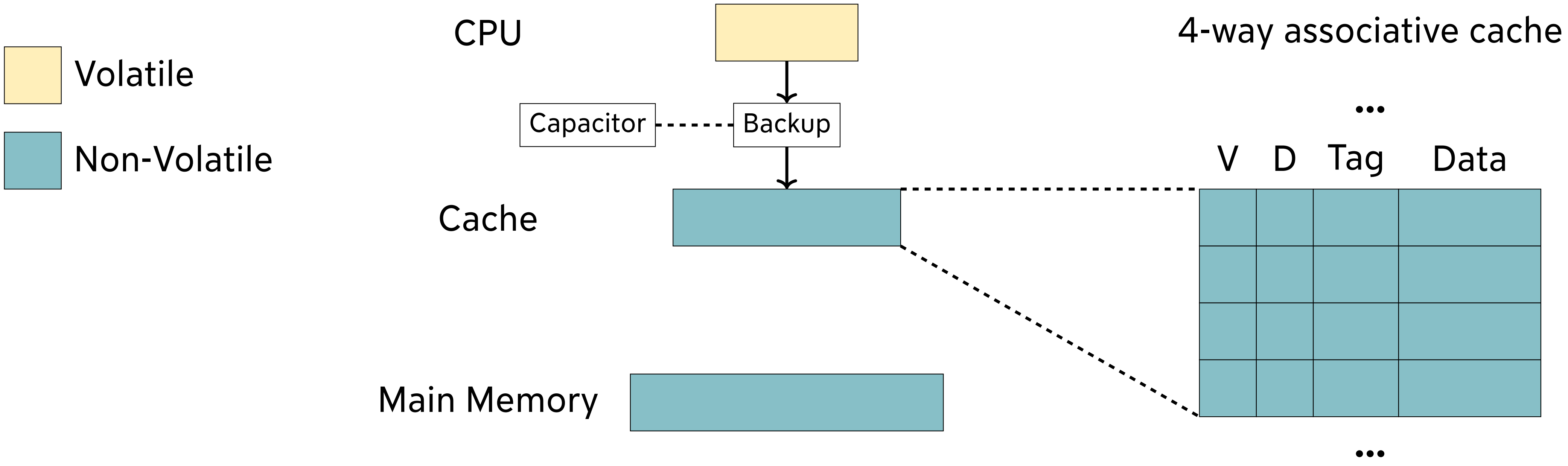




Volatile
Non-Volatile
CPU
Capacitor
Backup
Cache
Main Memory
4-way associative cache
...
V
D
Tag
Data
...



STT-RAM caches compared to conventional SRAM caches:

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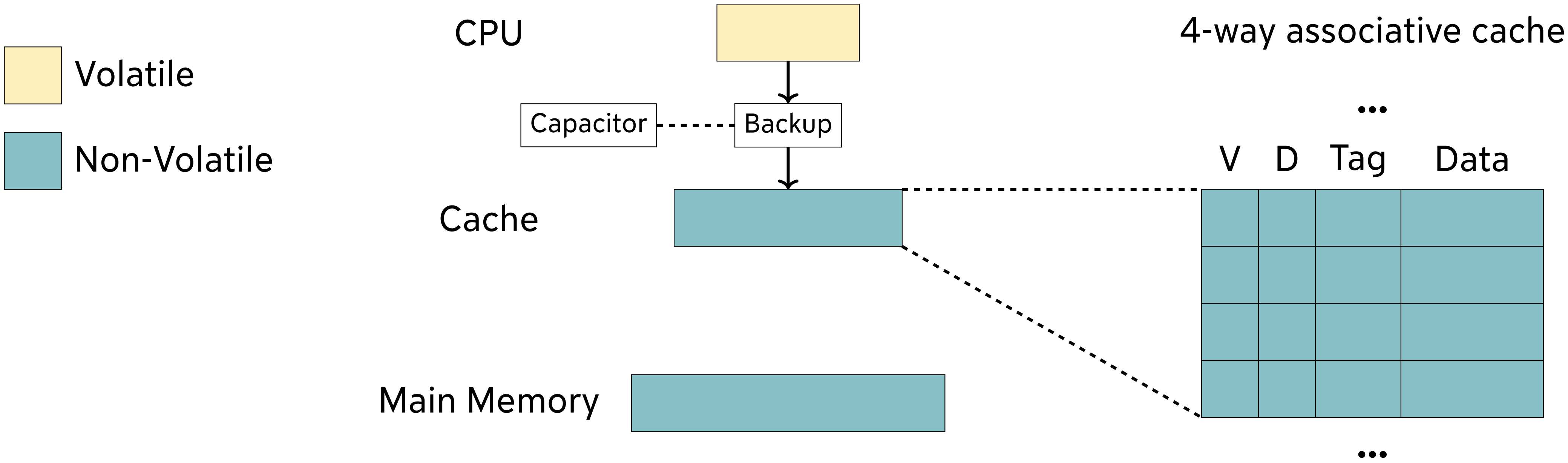

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- High write energy
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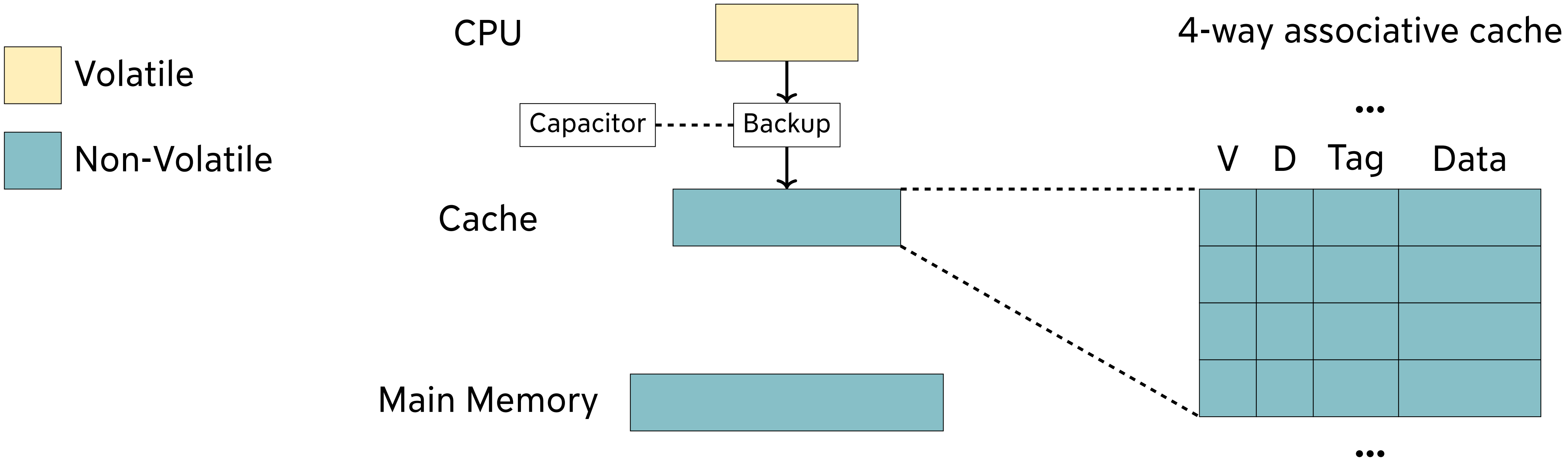

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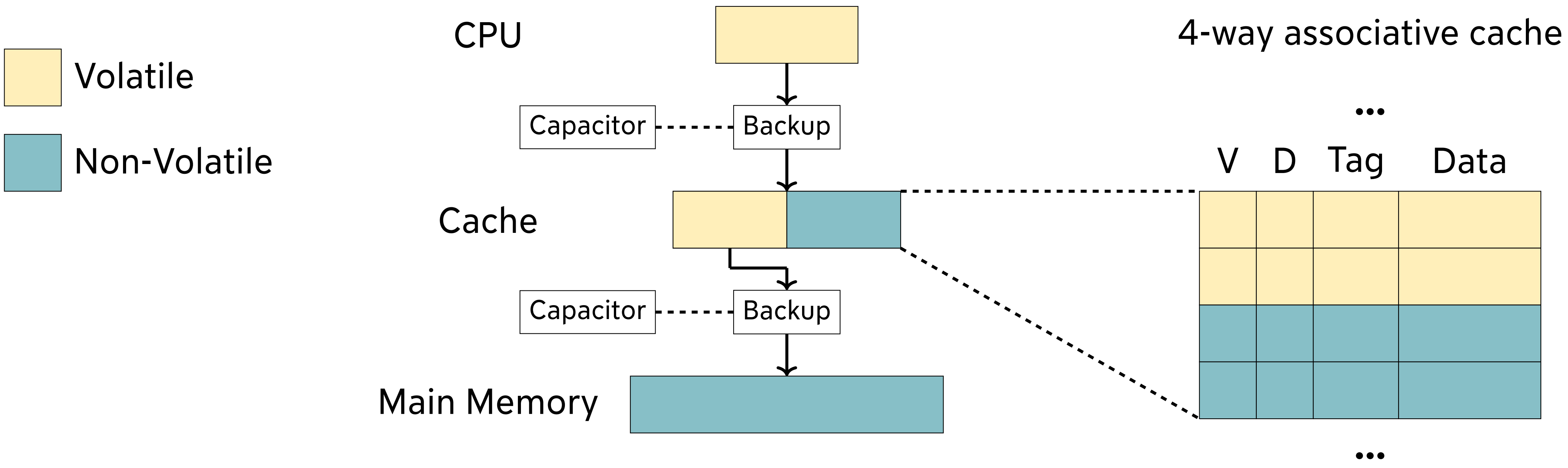
- + Low read energy
- + High density
- + Low static power



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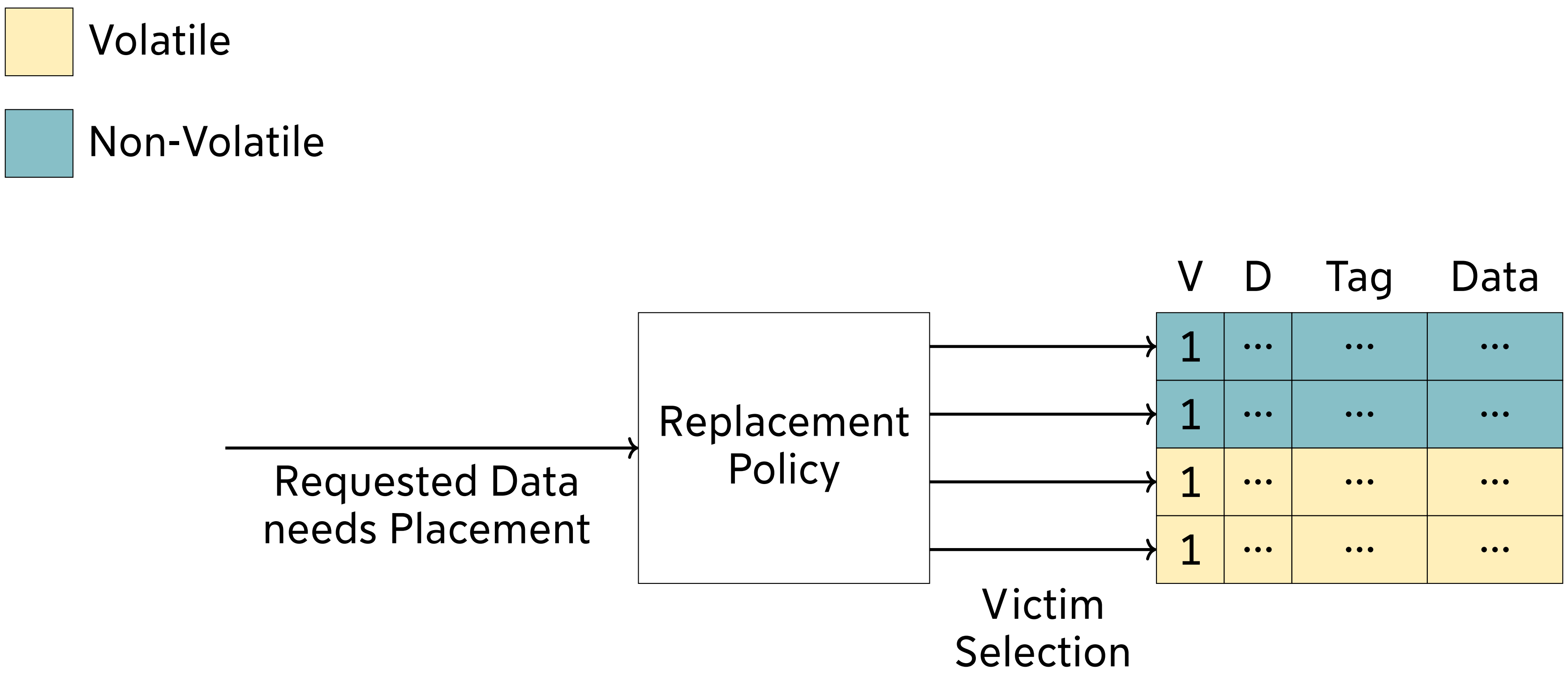

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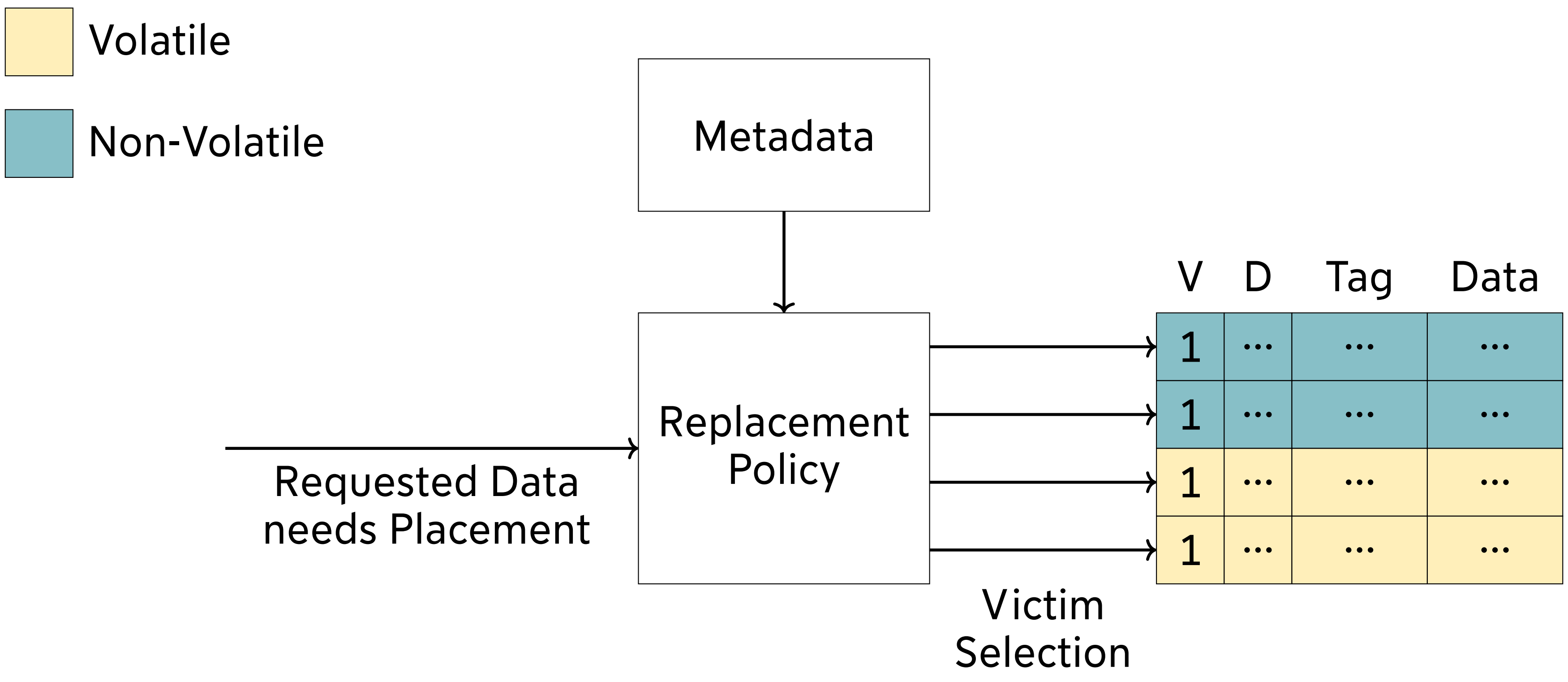

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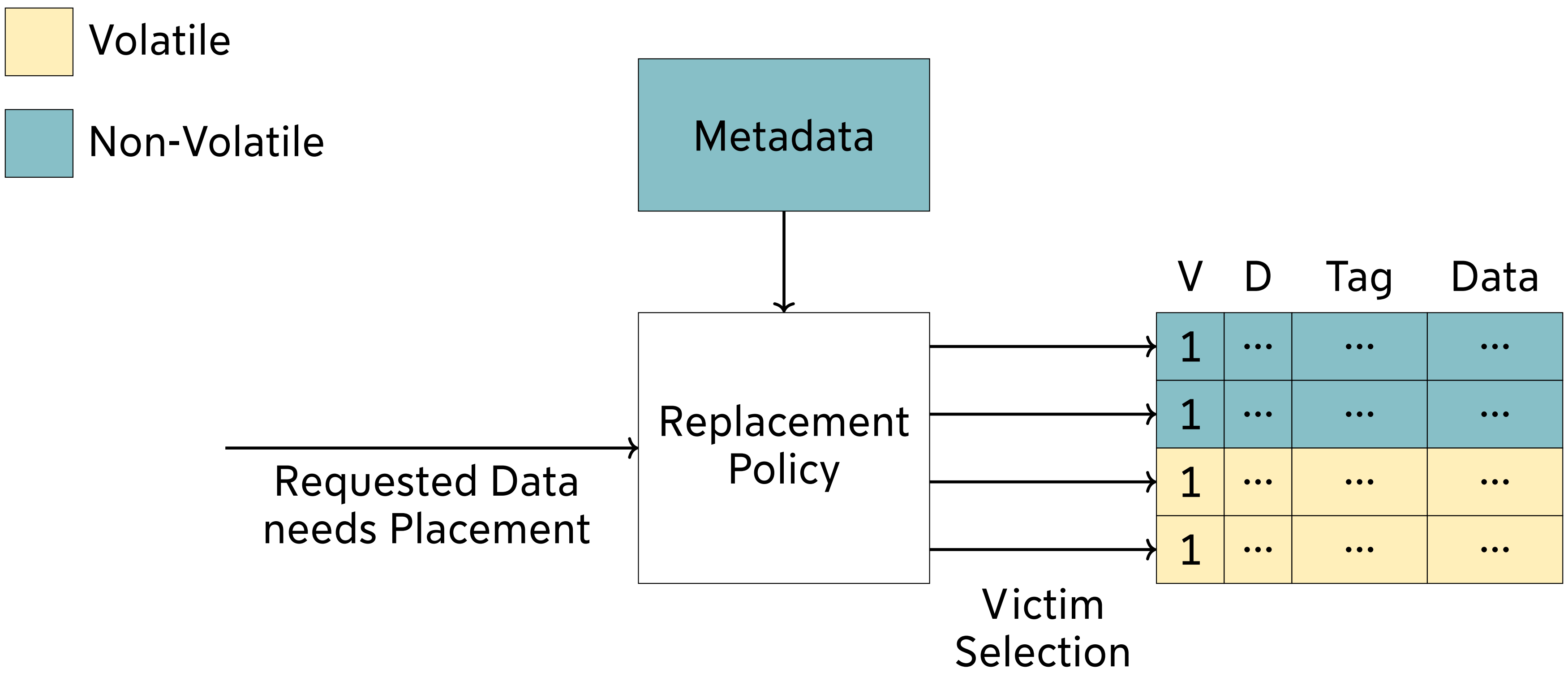

+ Keep previously acquired knowledge on, e.g., access patterns after a power outage
– Potential NVM endurance issues

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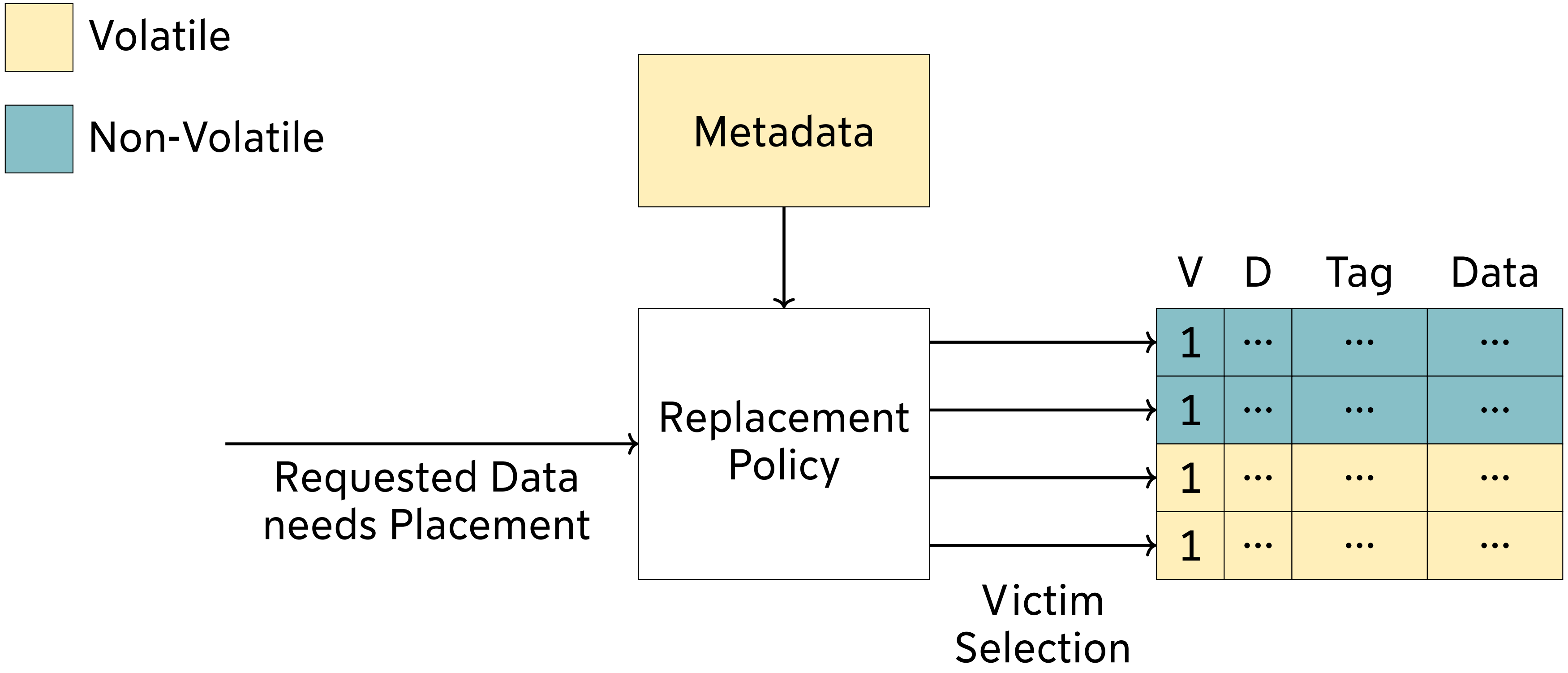

– Lose previously acquired knowledge on, e.g., access patterns after a power outage
+ Metadata reset following power outages as an opportunity to balance out accumulated mispredictions

Research Questions

- Is it worth considering this niche in the design space of hybrid caches?
- If so, is there a general rule on how replacement policy metadata should behave following a power outage?
- What does this imply for future and related research on hybrid caches for intermittent computing?

Round-Robin Replacement

	V	D	Tag	Data
	1	1	…	…
Next Victim →	0	0	…	…
	1	0	…	…
	0	0	…	…

- Pointer at next cache line (i.e., the next way in the cache set) to be replaced

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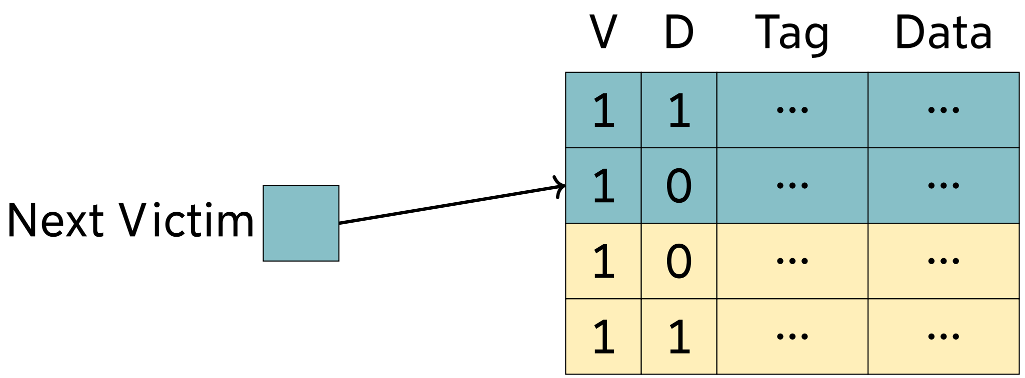
→ Supported by most ARM processors

Round-Robin Pointer Volatility

Non-Volatile Pointer

Volatile

Non-Volatile



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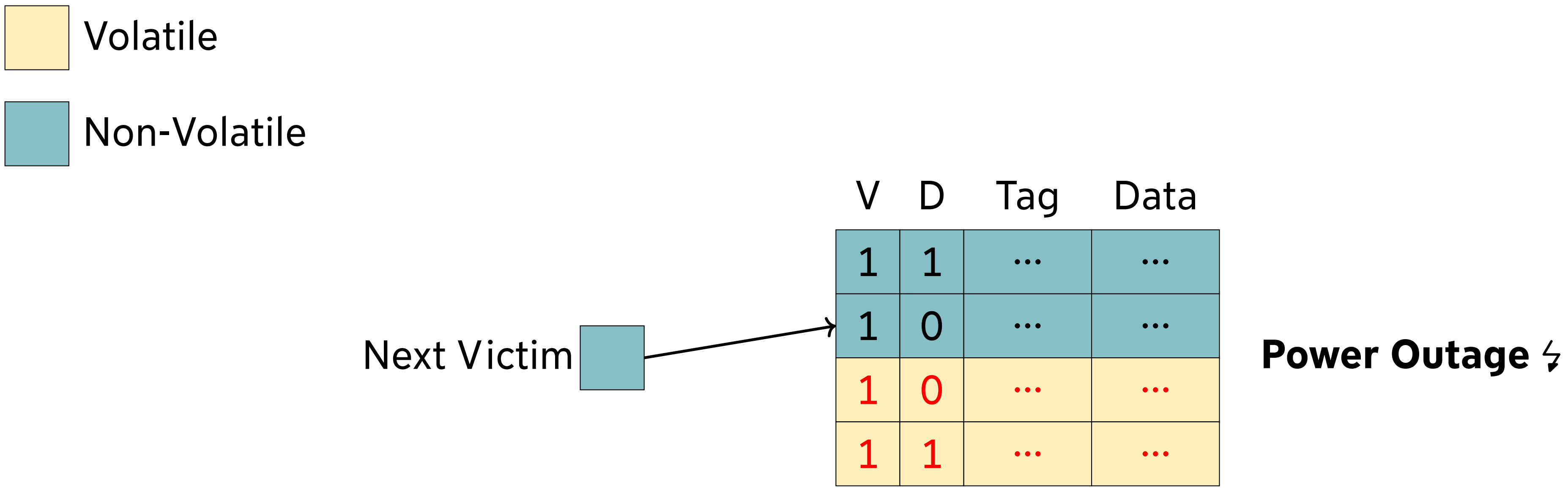

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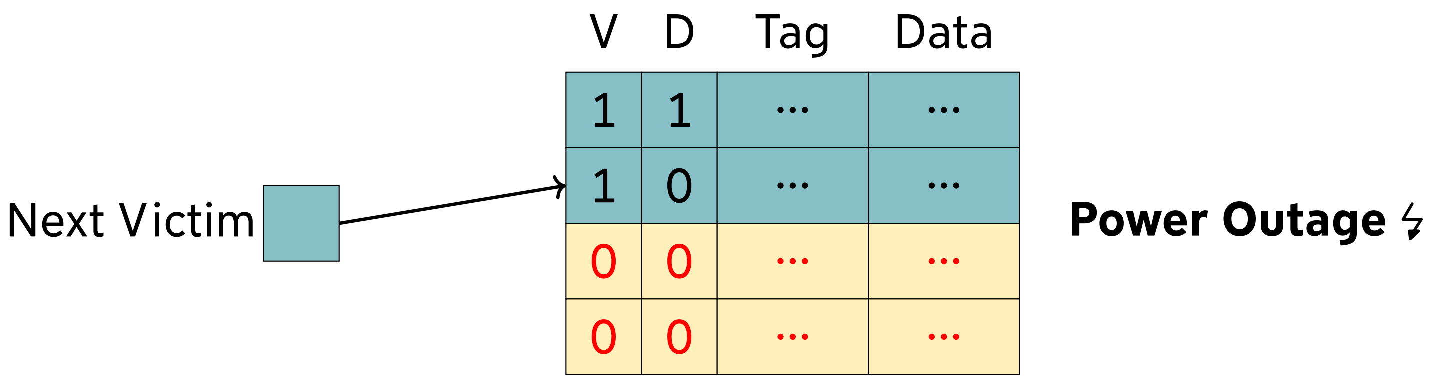

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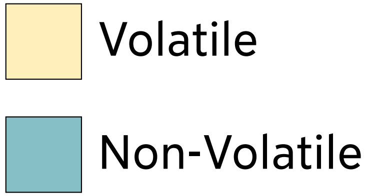

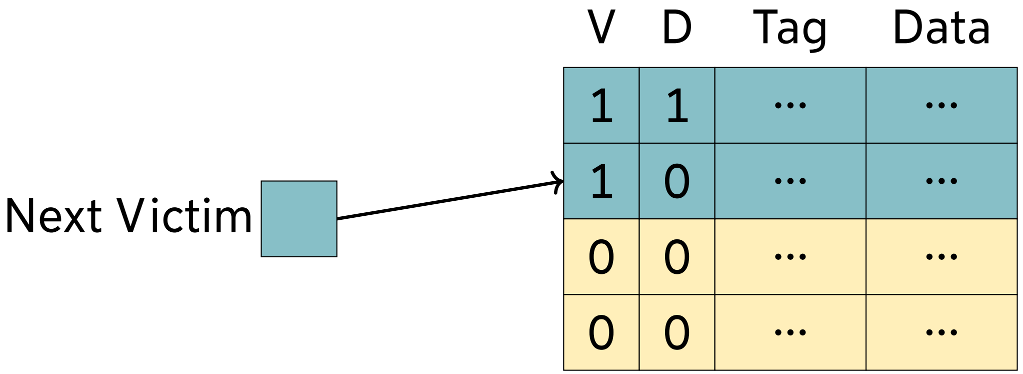

→ Invalid cache lines available, yet valid cache lines are chosen as the next victim

Round-Robin Pointer Volatility

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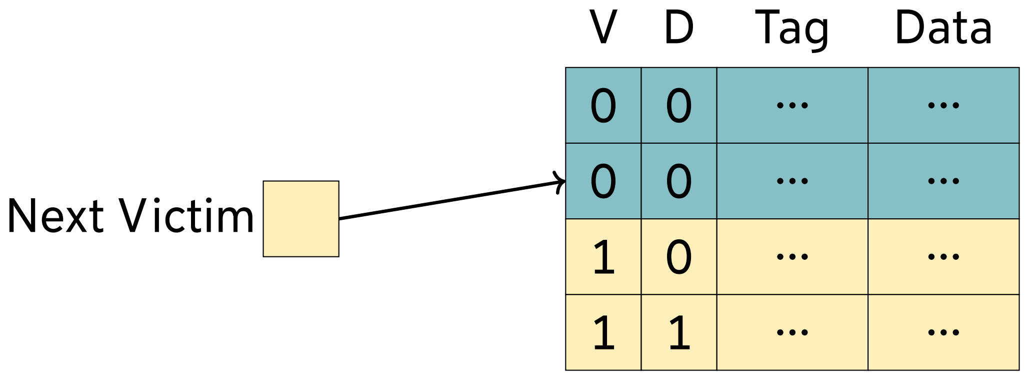

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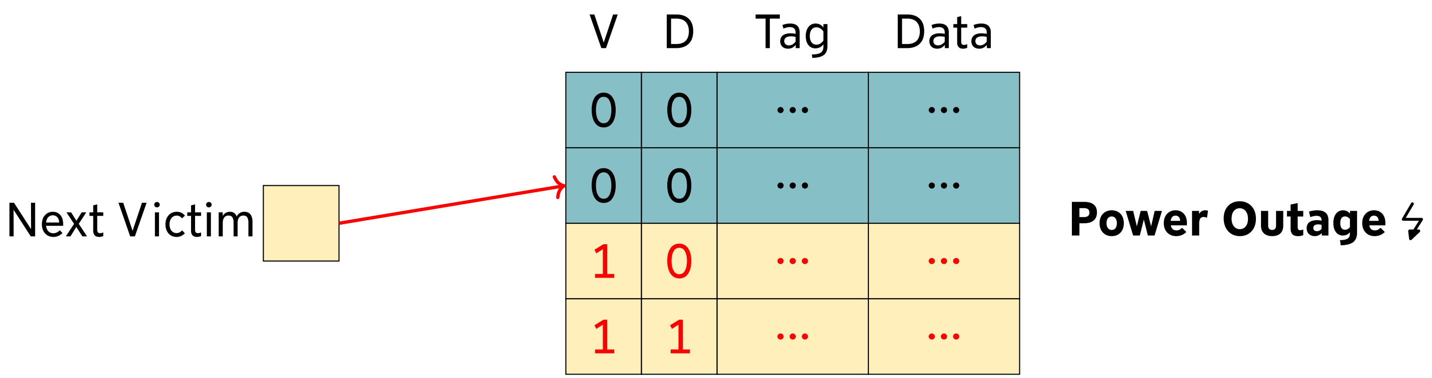

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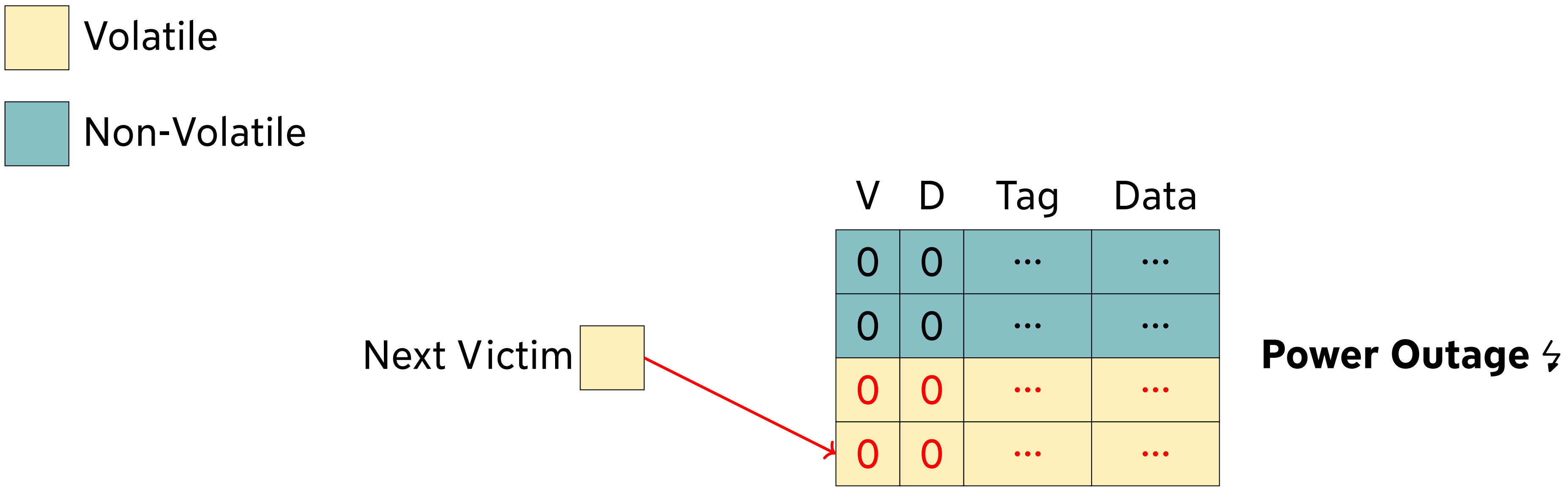

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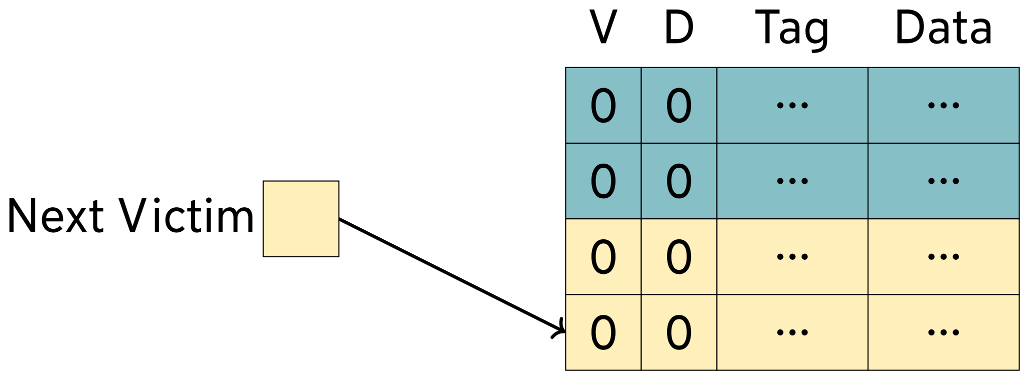

→ For small working sets and/or frequent power outages, non-volatile cache lines are not exploited

Experimental Setup

Architecture:

- Generic pipelined single-core out-of-order ARM CPU
- CPU clock of 240 MHz, system clock of 480 MHz
- 4-way associative 32 KB large SRAM/STT-RAM **hybrid data cache** (single-level)
- Cache parameters obtained using NVSim [Don+12]
- PCRAM main memory modeled after [Cho+12]

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Memory characteristics:

	Read Latency	Write Latency	Read Energy (per access)	Write Energy (per access)
SRAM Cache	2 Cycles @240 MHz	2 Cycles @240 MHz	0.009 nJ	0.009 nJ
STT-RAM Cache	2 Cycles @240 MHz	8 Cycles @240 MHz	0.007 nJ	0.056 nJ
PCRAM Main Memory	48 Cycles @400 MHz (tRCD)		0.081 nJ	1.685 nJ

Experimental Setup

Applications:

- Merge Sort *(write-intensive)*: Sort an input array containing 65,536 integers
- Image Processing *(read-intensive)*: 2D convolution on a 640×640 large image using a 3×3 large kernel

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Simulation Parameters:

- gem5 simulator [Bin+11] coupled with NVMain 2.0 [Por+15] to simulate non-volatile main memories
- A power outage is triggered every 2,500,000 CPU cycles
- Baseline architecture featuring a random replacement policy

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Objectives:

- Latency in clock cycles
- Dynamic energy consumption normalized to baseline architecture

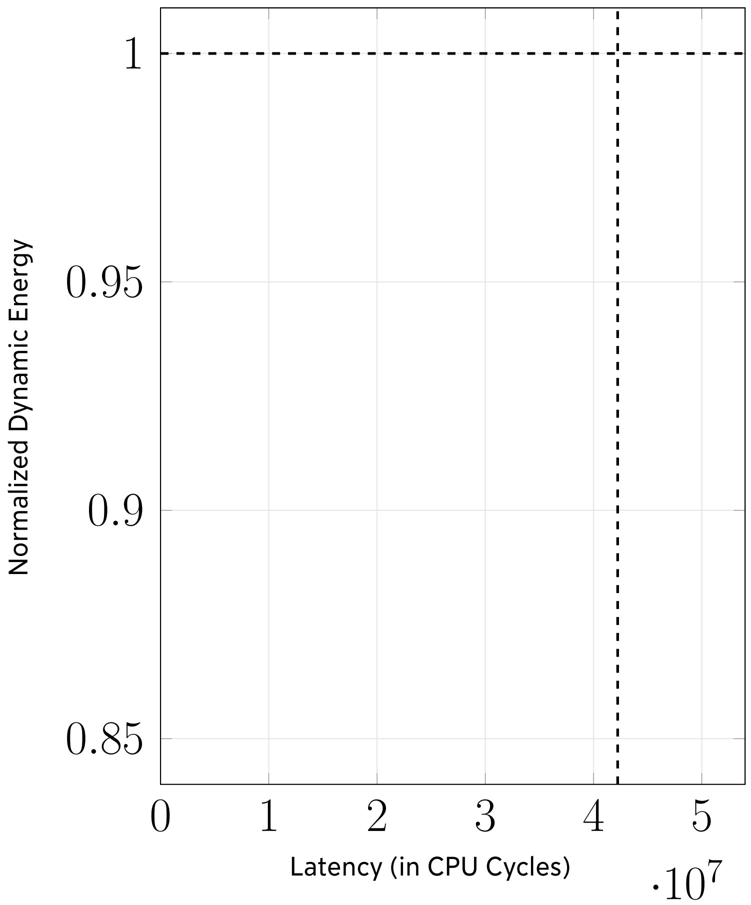
Goals Revisited

Analyze latency and energy trade-offs by comparing:

- A round-robin policy with a non-volatile pointer towards the next victim
- A round-robin policy with a volatile pointer that, following power outages, is reset to volatile cache lines

Experimental Results

Round-Robin (RR) Policy



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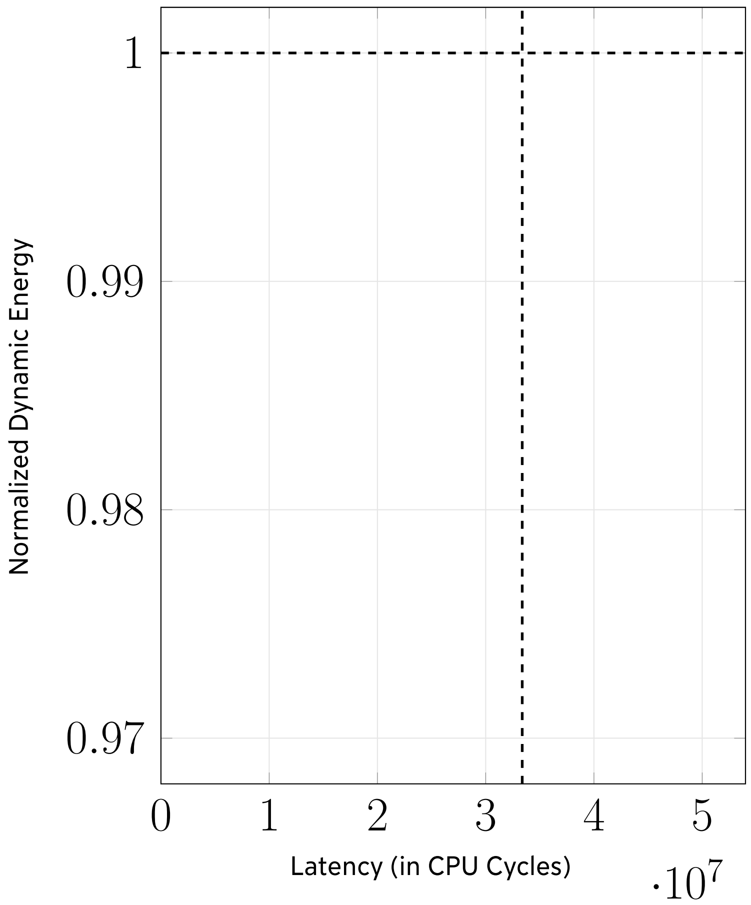

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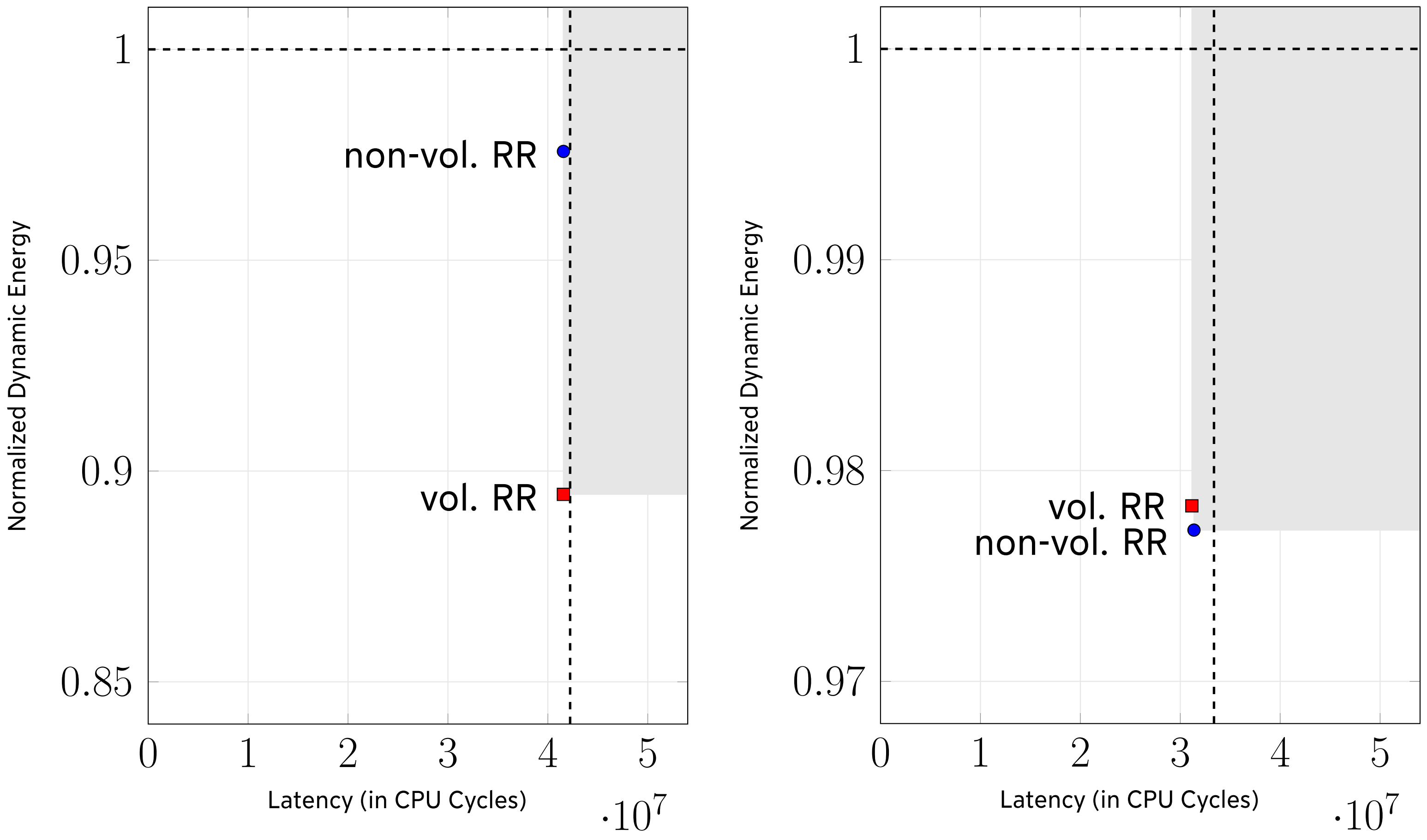
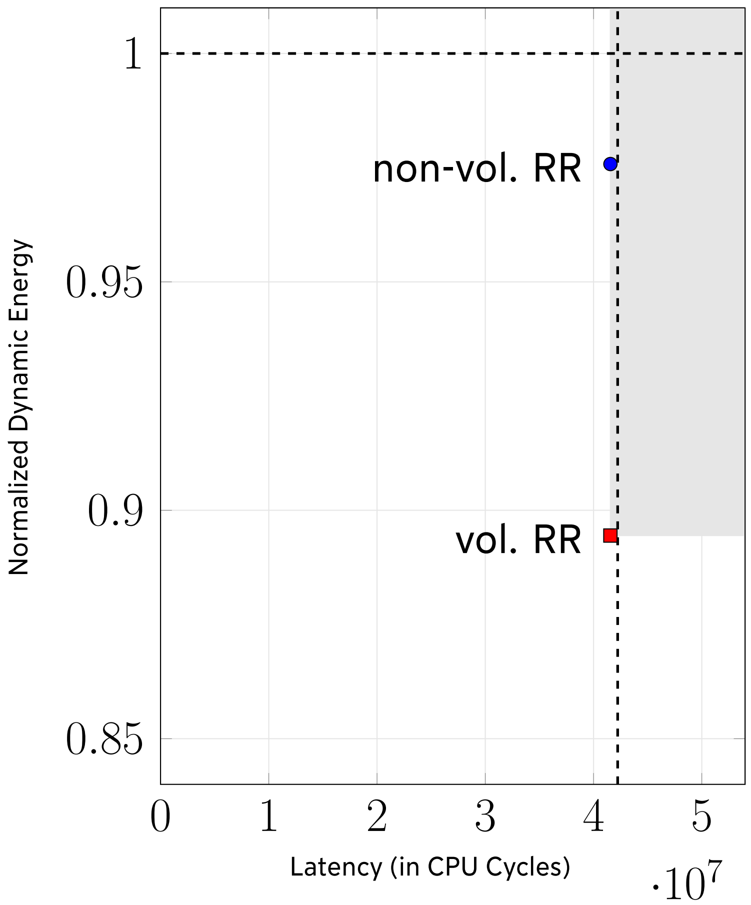


(a) **Merge Sort** (b) **Image Processing**



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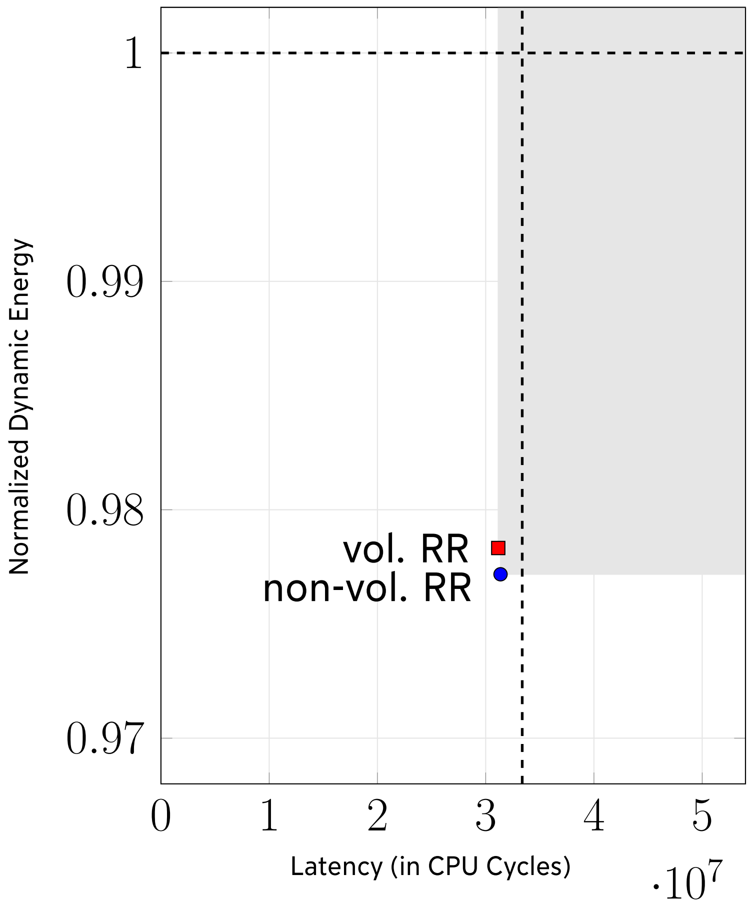

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Key takeaways:

- Both volatility options outperform a randomized approach
- The two RR approaches do not dominate each other

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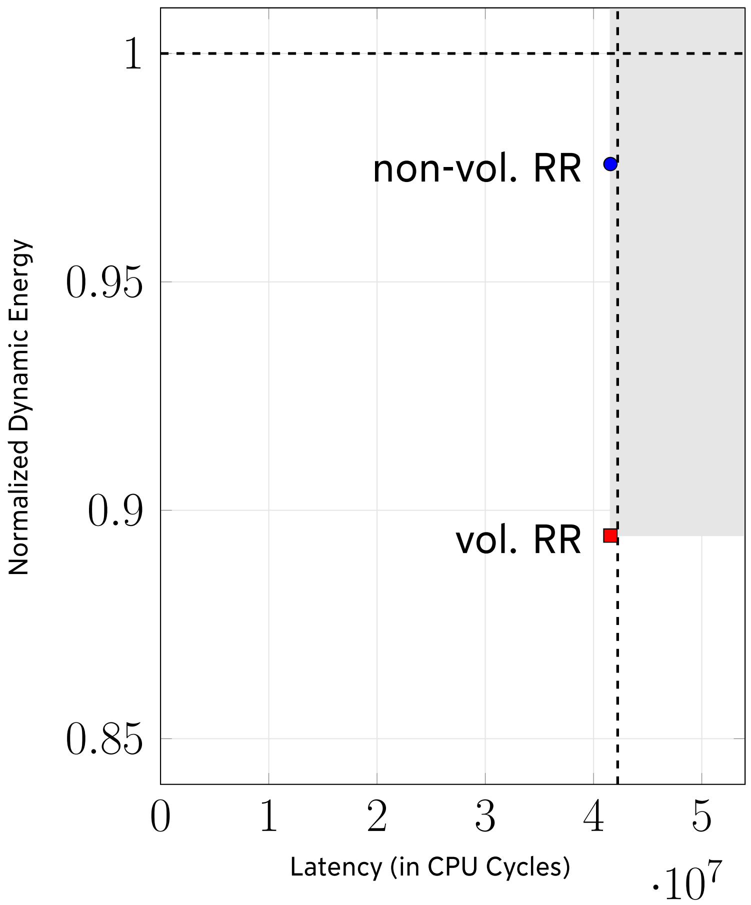

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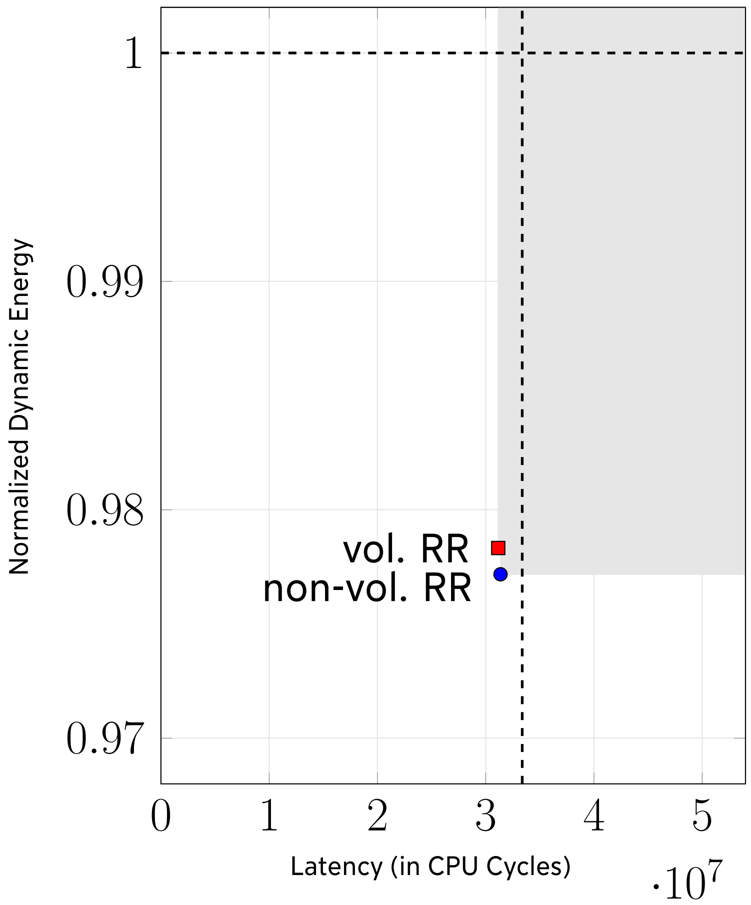

(b) **Image Processing**

Key takeaways:

- Both volatility options outperform a randomized approach
- The two RR approaches do not dominate each other
- Volatile RR pointer leads to accesses mainly revolving around the volatile section
- Up to 8.4% difference in dynamic energy consumption depending on the volatility of the RR pointer

Write Intensity Prediction [AYC16]

At each Program Counter (PC), the invoked data accesses can lead to a cache miss, with future cache hitting accesses to this cache line being either...

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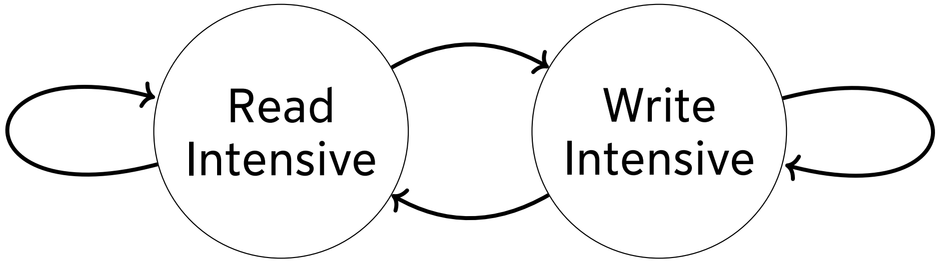

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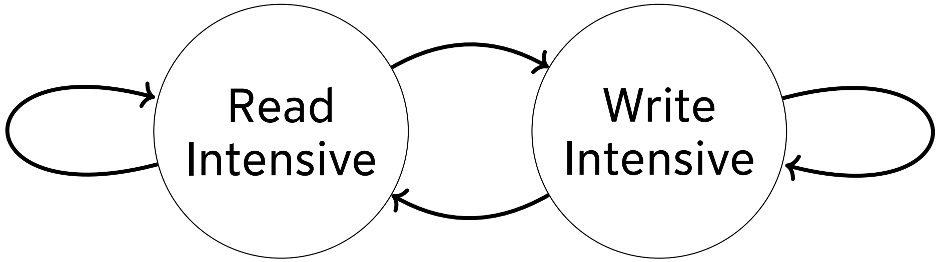


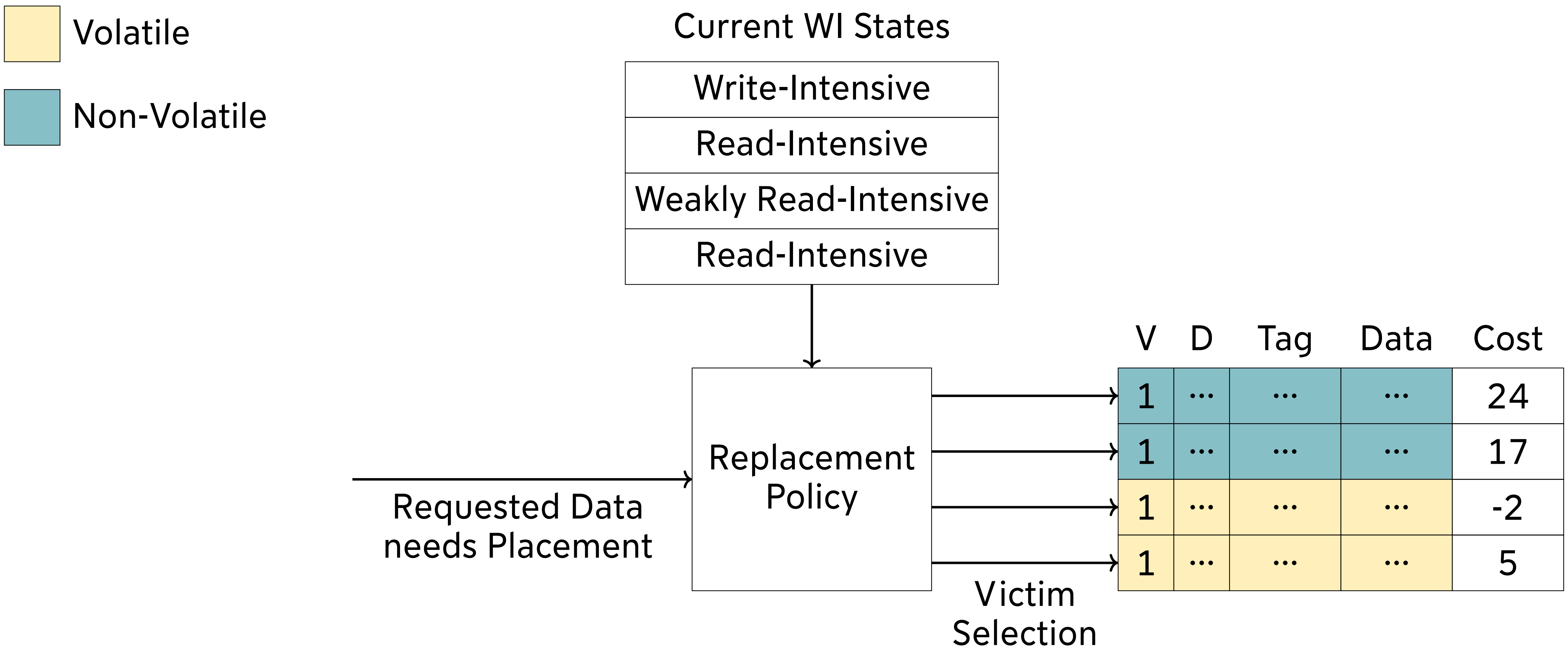
Write Intensity (WI) Policy fundamentals:

- Predict write intensity to suitably place data in either the volatile or non-volatile cache section
- **State table:** Contains current state for all state machines

→ Add "Weakly Write-Intensive" and "Weakly Read-Intensive" states

- **Costs:** Track accesses to cache line. Used to update state machine on eviction

Candidates for Different Technological Implementations



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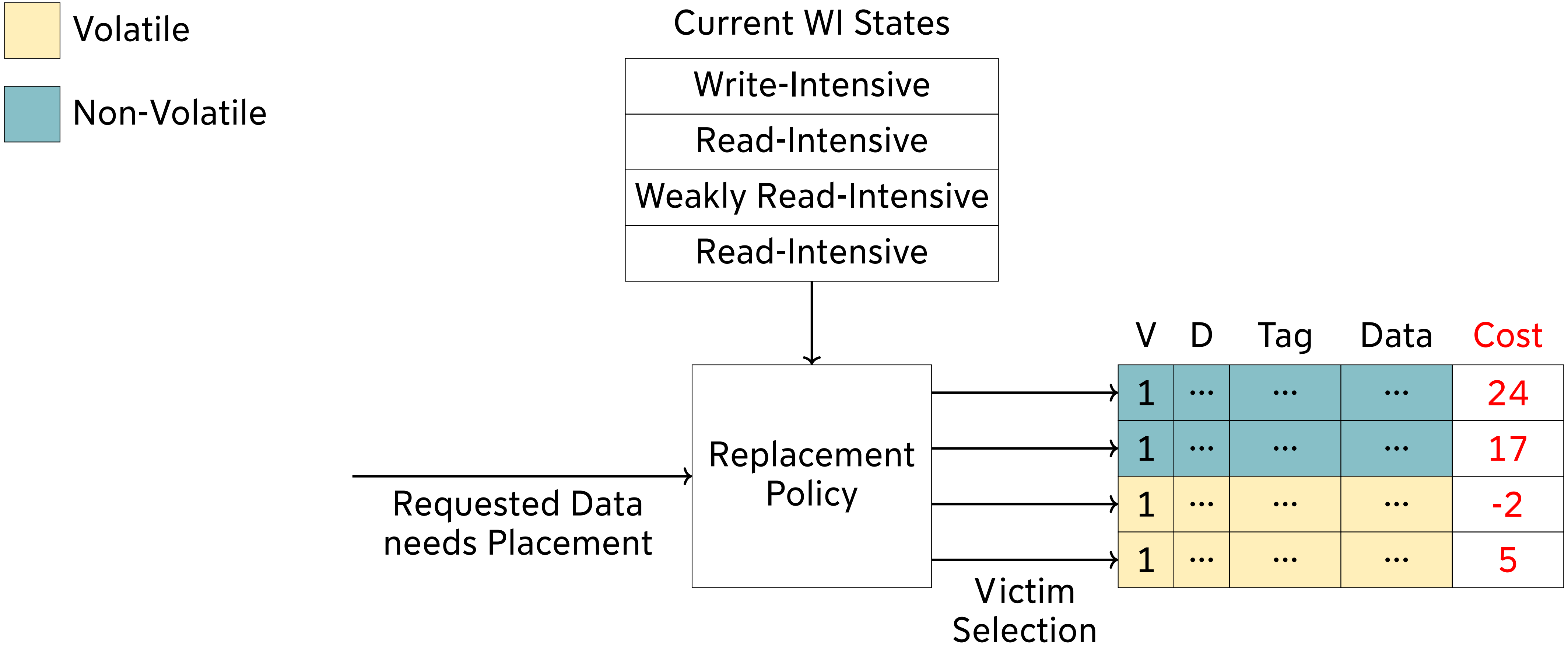

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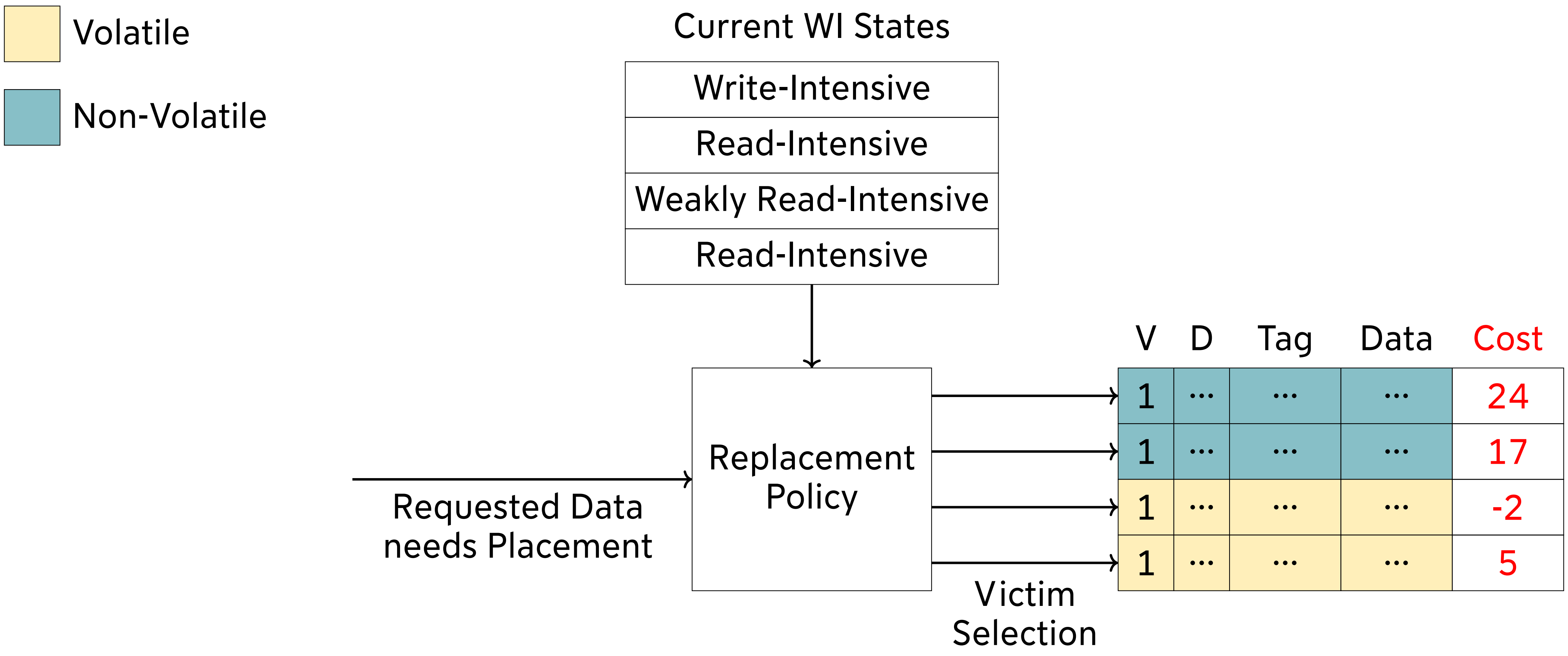

Cost field updated on every access to respective cache line
→ Many writes, thus unsuitable for NVM implementation (endurance issues)

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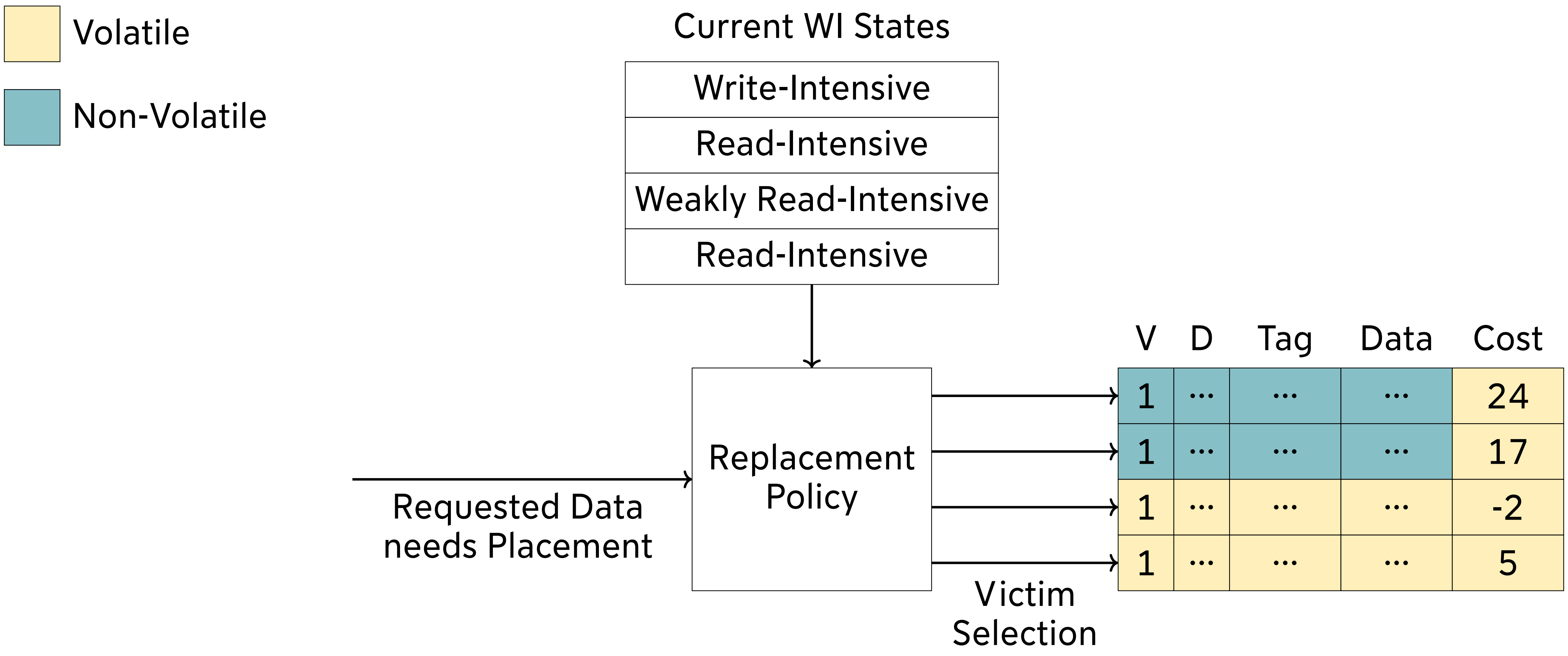

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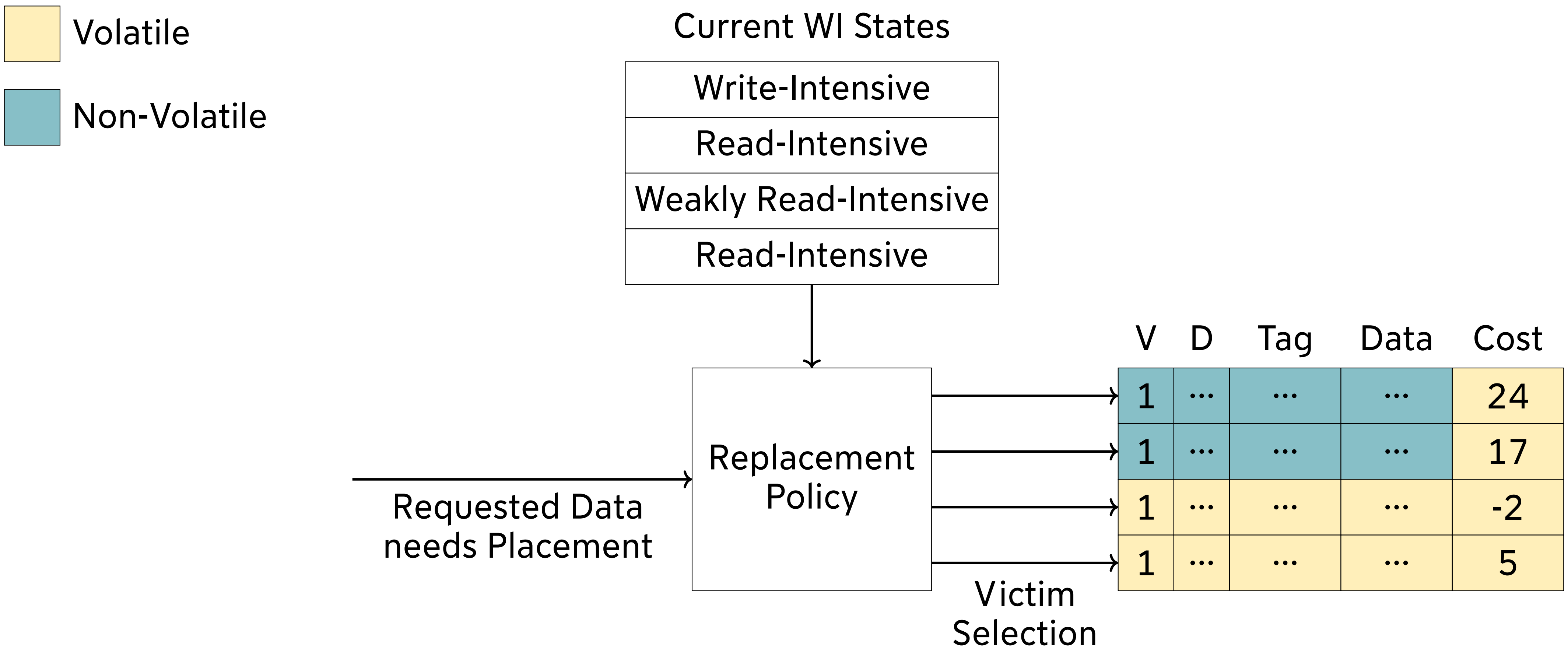

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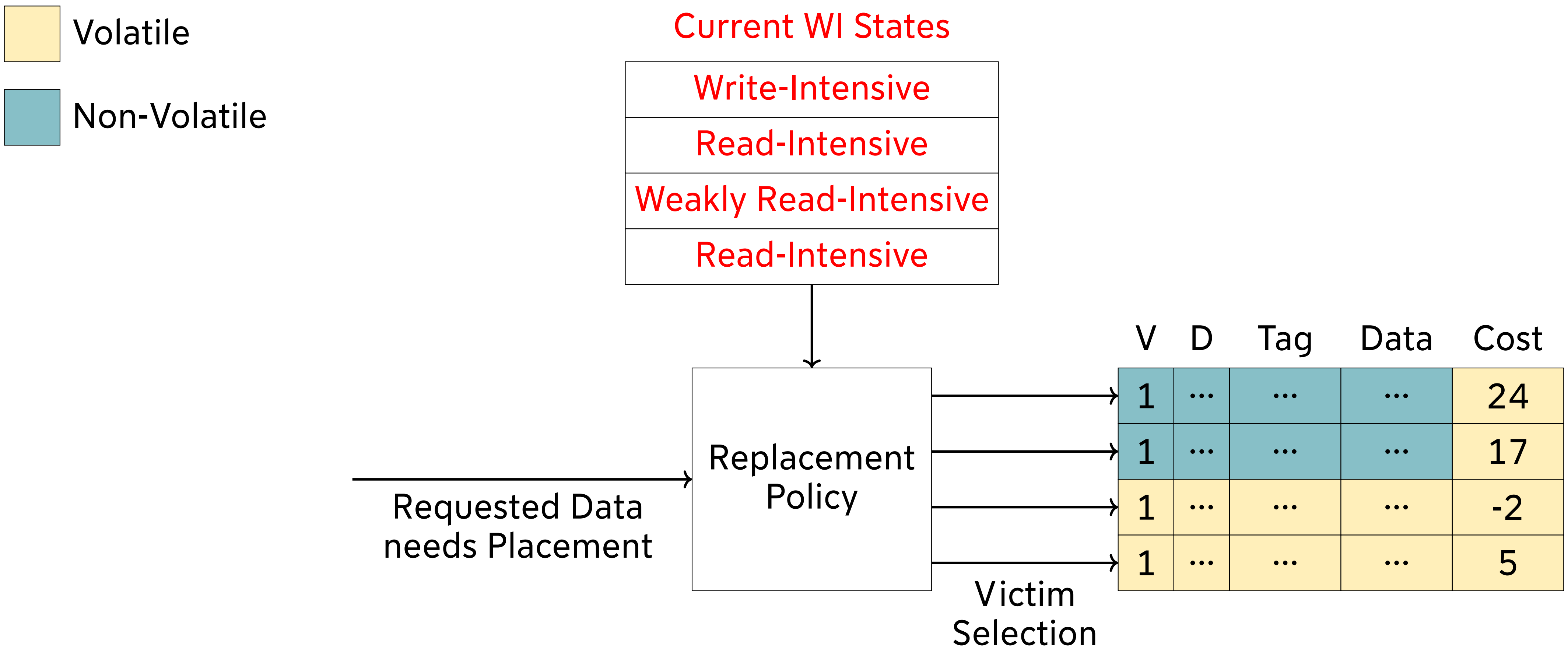

WI states updated on eviction (transition determined by cost function)

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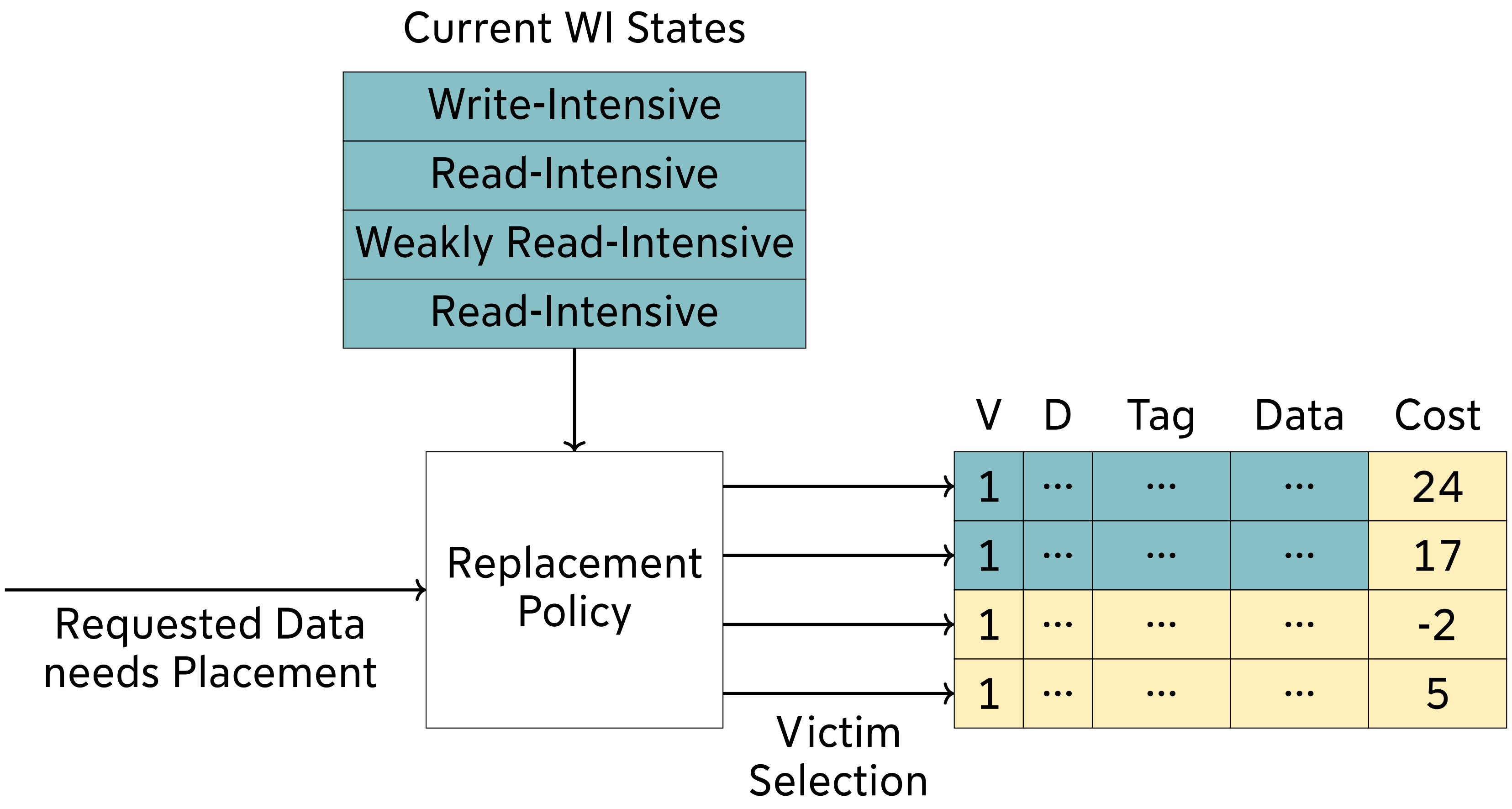

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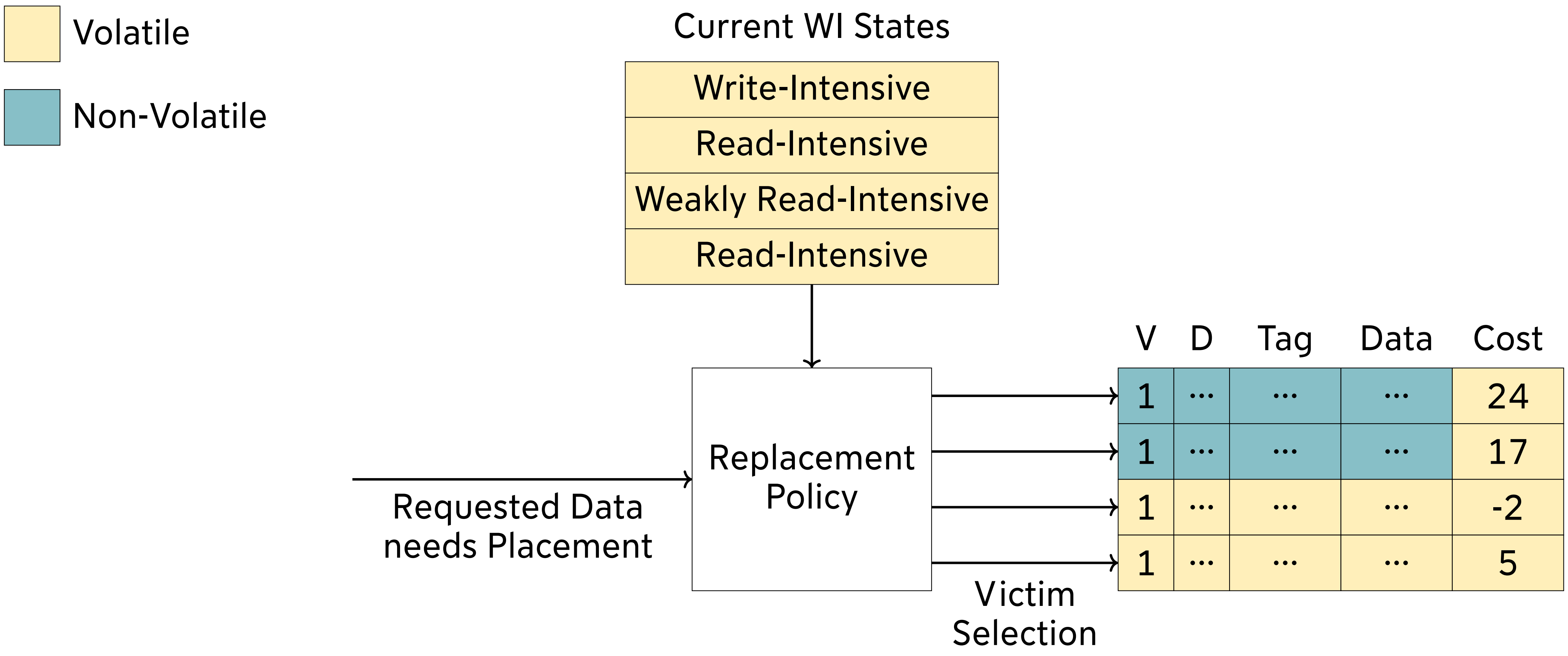

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→ Volatile implementation to reset all state machines to one of the 4 WI states (depending on state encoding)

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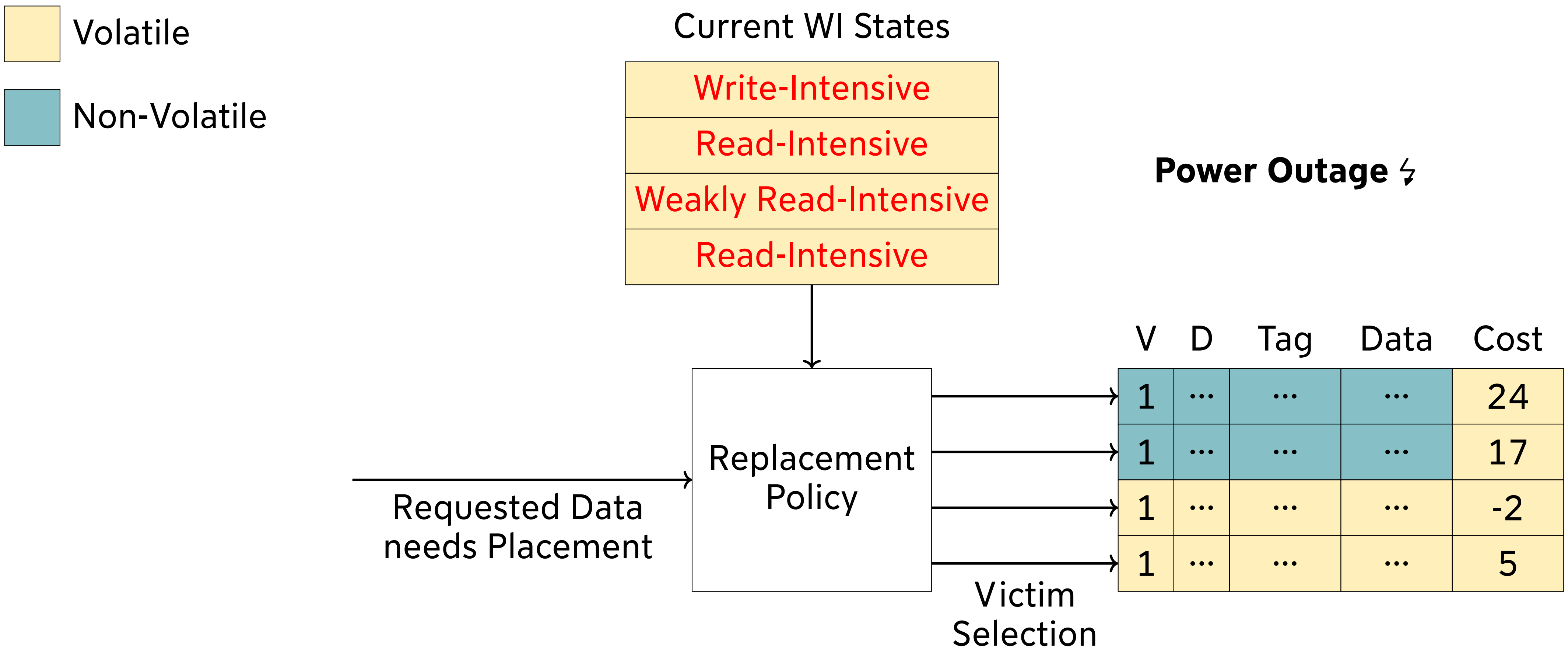

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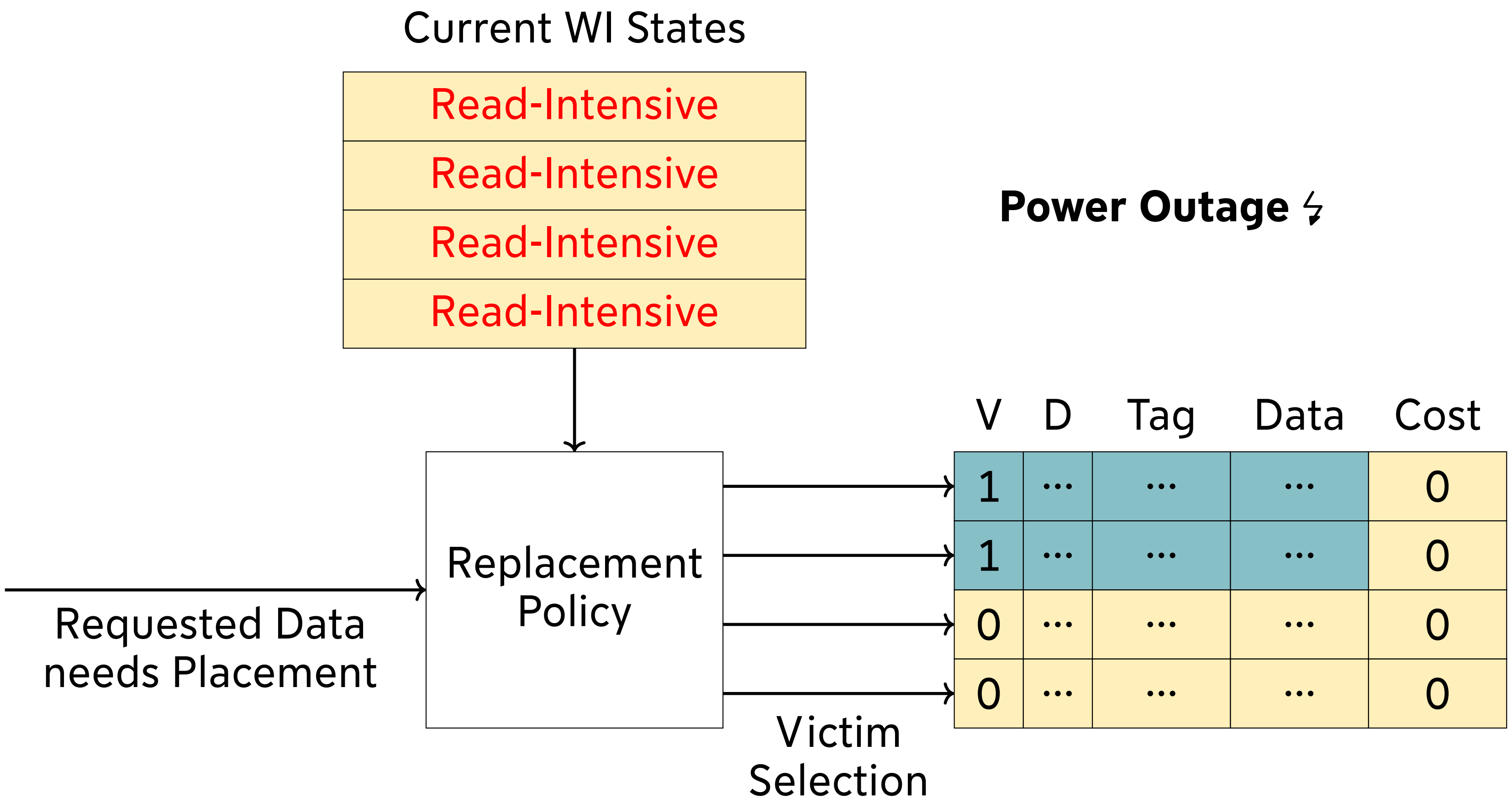

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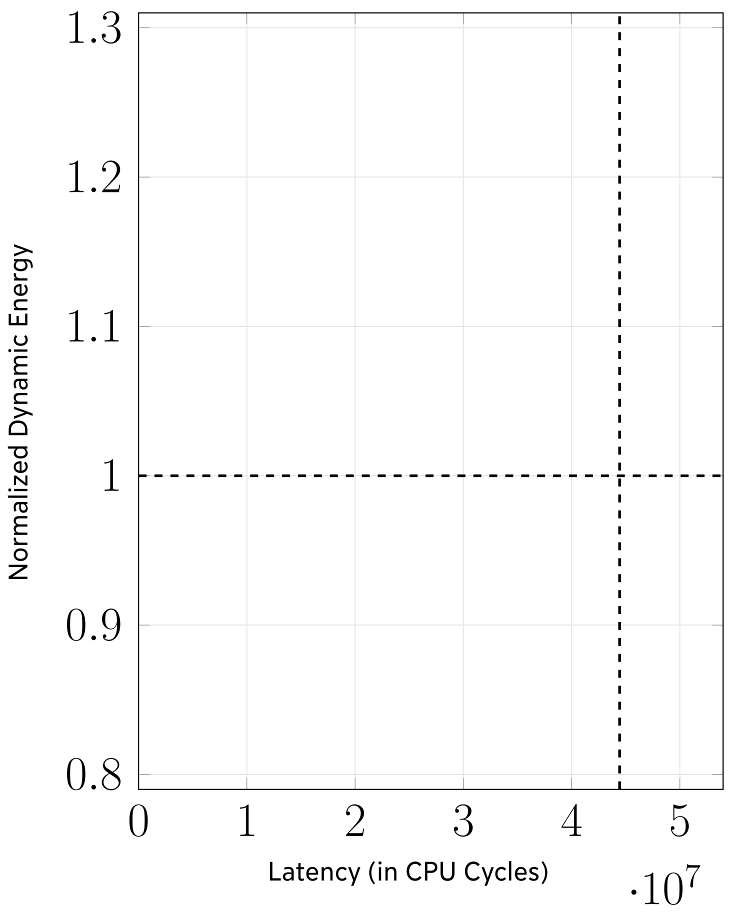
Goals Revisited

Analyze latency and energy trade-offs by comparing:

- A WI policy with a non-volatile state table (here, serving as the baseline)
- A WI policy with a volatile state table and different state encodings resetting all state machines to either
  - the Read-Intensive (RdI) state
  - the Weakly RdI state
  - the Write-Intensive (WrI) state
  - the Weakly WrI state

→ 5 different comparison points



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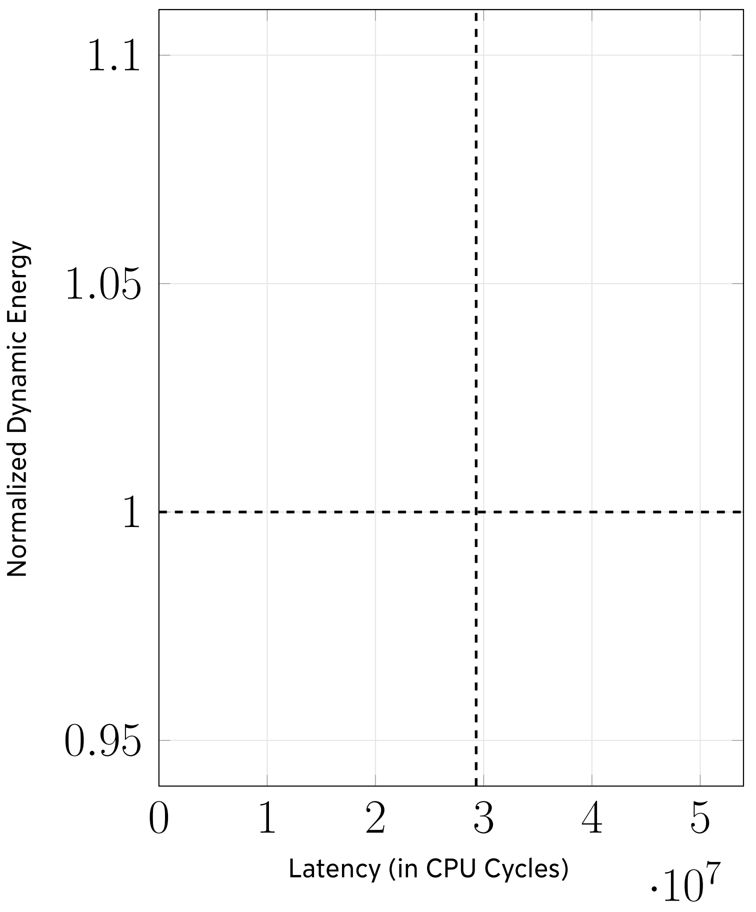
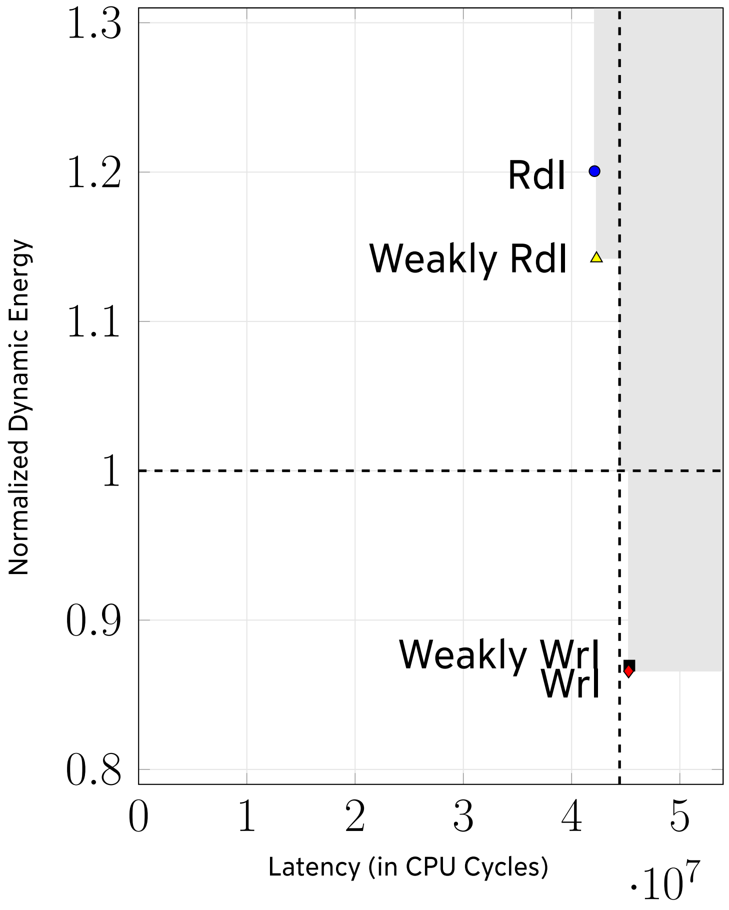


(b) **Image Processing**

Experimental Results
WI Policy



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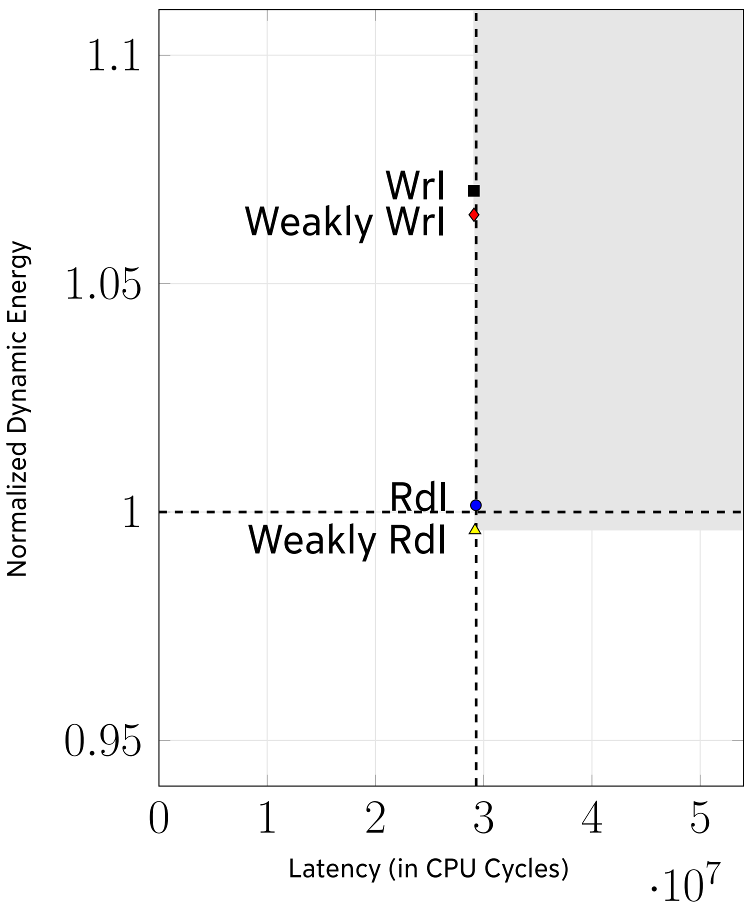

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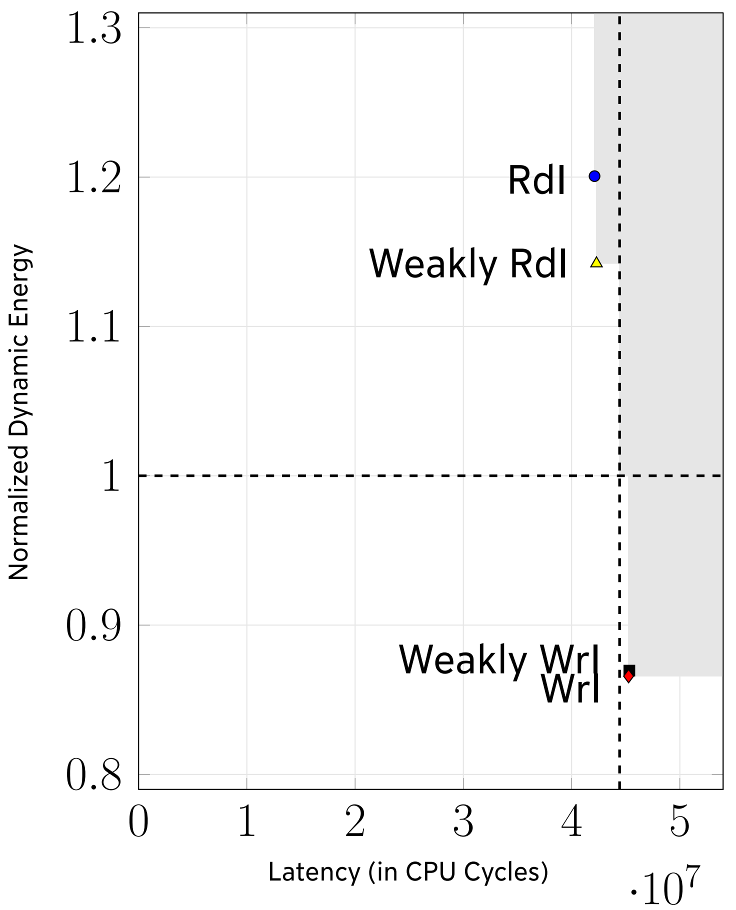

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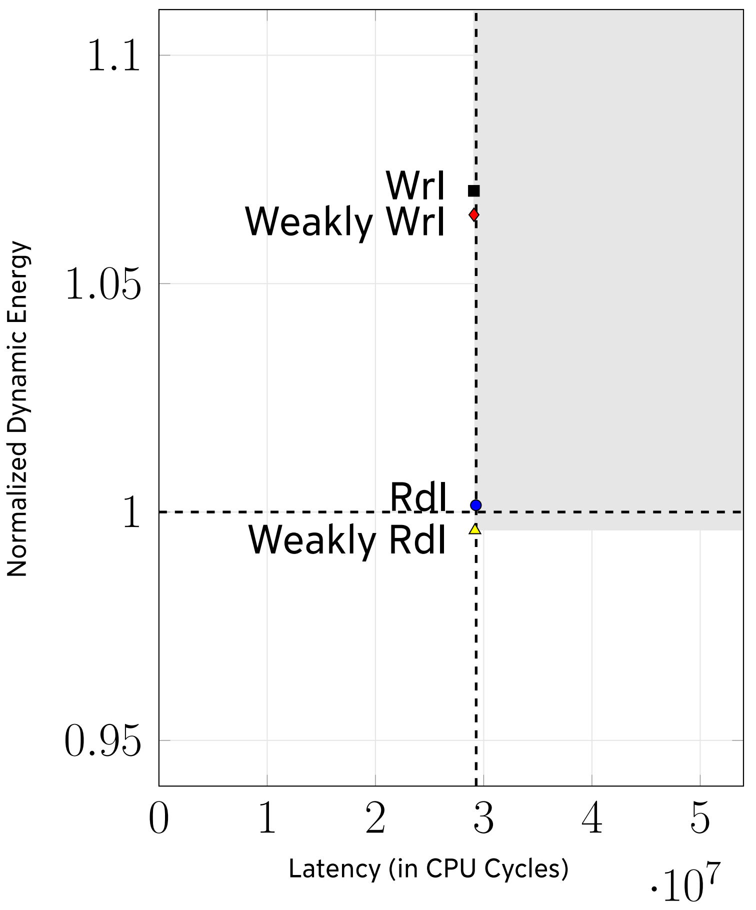

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Key takeaways:

- State-machines tend to drift towards the read-intensive side following power outages

→ Harmful for write-intensive application

Experimental Results

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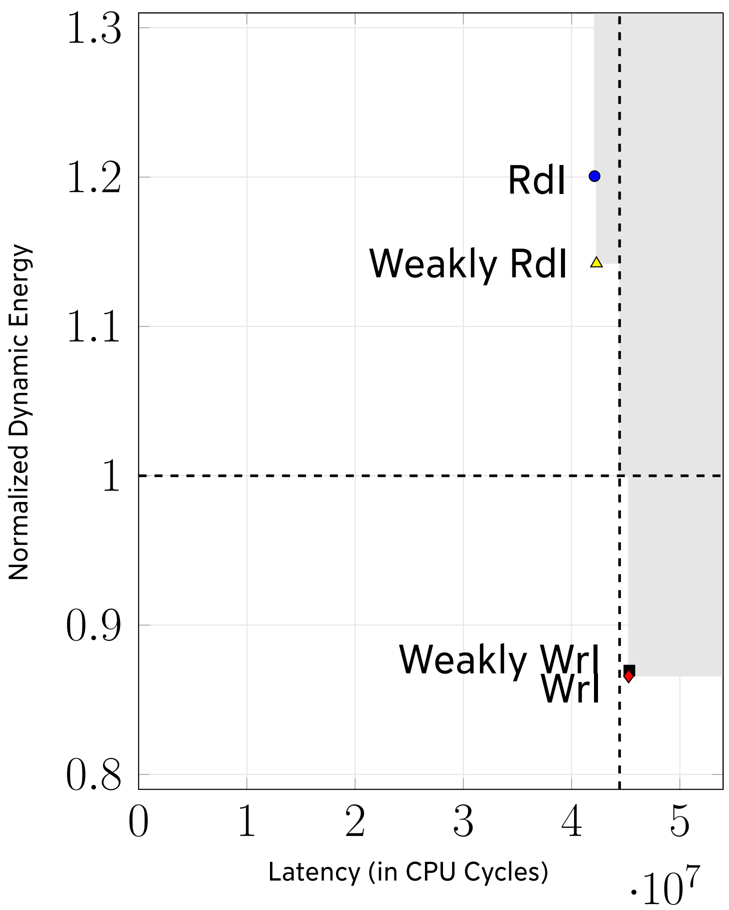

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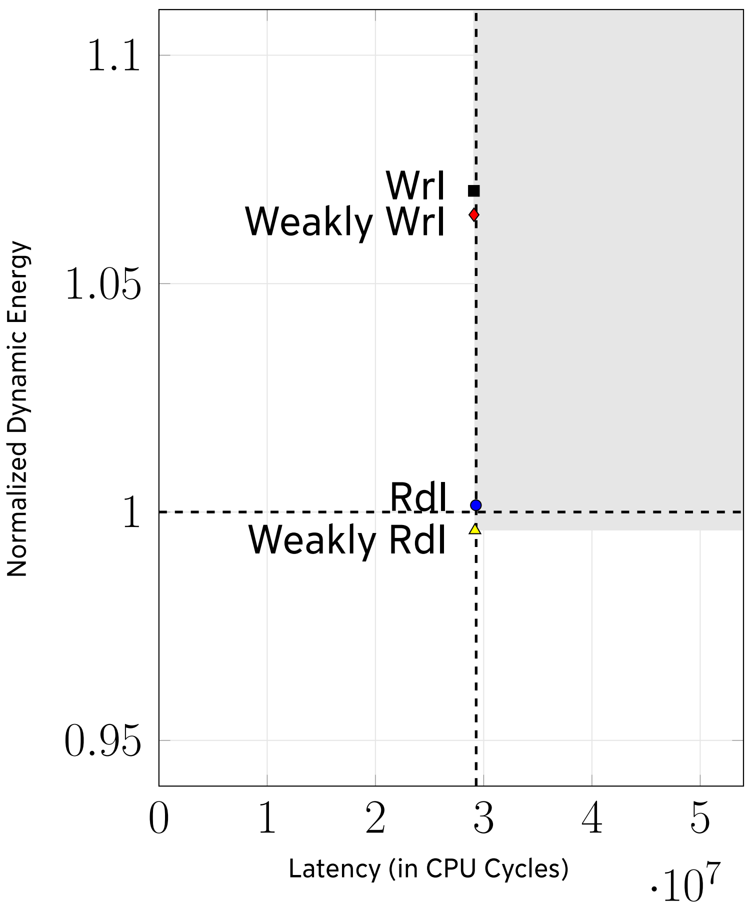

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Key takeaways:

- State-machines tend to drift towards the read-intensive side following power outages

→ Harmful for write-intensive application

- Resetting state machines after power outages can counter mispredictions
- Most suitable reset state depends on application characteristics

→ State encoding can make up to 28% difference in dynamic energy consumption

Conclusion and Outlook

- To keep or not to keep? No general consensus regarding the ”best” option for implementing policy metadata
- However, it’s an important design decision: We have seen up to 28% difference in energy consumption by switching to a different approach of implementing replacement policy metadata

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→ When developing new policies: Evaluate different options for technologically implementing their metadata to unlock additional potential in energy/latency savings

→ Knowing about the characteristics (write intensity) of your applications, helps to realize better design decisions

→ Do not undermine the role of niches in the design space

Thank you for your interest and attention!

Any questions?

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